Visvesvaraya Technological University, Belagavi

MODEL QUESTION PAPER

3rd Semester, B.E (CBCS 2017-18 Scheme) EC/TC

Course: 17EC34- Digital Electronics, *Set no. 2*

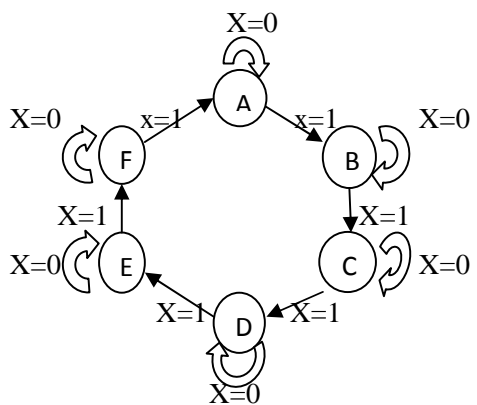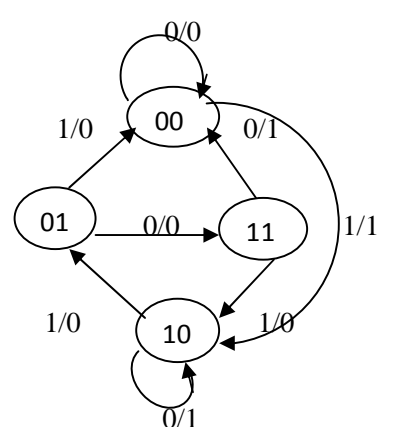Time: 3 Hours   Max. Marks: 100

Note: (i) Answer Five full questions selecting any one full question from each Module.

(ii) Question on a topic of a Module may appear in either its 1st or/and 2nd question.

		MODULE-1	**MARKS**
1	a.	Define the following (i)Essential prime implicant (ii)cannonical SOP (iii)cannonical POS (iv) incompletely specified functions	4M
	b.	Using K-map determine the minimal POS Expression and realize the simplified expression using NAND gates f(a,b,c)=π(0,1,4,5,6,7,9,14)+D(13,15)	8M
	c.	Simplify the following Expression using K-map T= $\bar{v}\bar{w}$ +$\bar{v}$ w$\bar{y}$ +v $\bar{w}$z	8M
		OR	
2	a.	Simplify the given Boolean Function using Quine-Mcluskey method y =$\sum m$(1,3,8,6,10,12,14) +dc(7,13)	8M
	b.	Convert the following Boolean function into mintermcannonical form y =f (a,b,c)=(a+b)(a+c)	4M
	c.	Design a 3input,1 output minimal Combinational network that has a logical-1 output when the majority of its inputs are logic-1 and has a logic-0 when majority of inputs are logic-0	8M
		MODULE-2	

3	a.	Implement the following function using 74138 Decoder
		
		    a) f(a,b,c) = πM(2,3,4,5,7)
		    b) f2(a,b,c) = $\sum m$(1,3,5)
			4M

	b.	What is Magnitude Comparator? Design 2 bit Comparator by writing TT, Expression and logic diagram	10M
	c.	What are the problems with basic Encoder? Explain 8 to 3 priority Encoder with basic Encoder	6M
		OR	

4	a.	Implement f(a, b, c ,d) =$\sum m$(0,1,5,6,7,10,15) using 8:1 MUX with a, b, c as select lines	5M
	b.	Explain 4bit Carry look ahead Adder with neat diagram and Relevant Expressions	10M
		MODULE-3	
5	a.	Explain the Operation of a Switch debouncer built using SR latch with the help of circuits and waveforms	8M
	b.	Explain MS JK flip-flop with the help of circuit diagram and waveforms	8M
	c.	Define (i) Setup Time (ii) Hold Time (iii) Propagation Delay (iv) Function Table	4M
		OR	
6	a.	Explain Positive Edge Triggered D Flip-flop with the help of circuit diagram and waveforms	8M
	b.	Obtain the Characteristic Equations for the following Flip-flops (i) JK (ii) SR	6M
	c.	Explain 0's and 1's Catching problem in Pulse Triggered MS JK Flip-flop with the help of timing diagram	6M
		MODULE-4	
7	a.	Design 3 bit synchronous Up Counter using JK Flip-flop write Exitation table transition table and Logic diagram	10M
	b	Describe the working of Universal Shift Register with the help of register operation and mode control table	10M
		OR	
8	a.	Explain the working Principle of 4 bit Ripple Binary Counter using the Edge Triggered T Flip-flop. Also draw the Timming Diagram	8M
	b.	Explain the MOD 8 Twisted Ring Counter with the help of Logic Diagram, Truth Table	4M
	c.	Write State Diagram for MOD 5 self correcting counter and briefly explain. The sequence is 000,001,101,110,111,000	8M
		MODULE-5	

9	a	Design a Counter circuit JK Flip-flop for the following sate table. follow the standard steps for design X is Enable for up counting use state alignment: A=000 B=010 C=011 D=101 E=110 F=111	10M
	b.	Construct melay state diagram that will detect input sequence 10110, when input pattern is detected . 2 is asserted high give state diagram for each sate.	10M
		OR	
10	a.	Design a sequential circuit for s state diagram shown below	12M
	b	Distinguish between moore and melay model with necessary block diagram	6M
	c.	What is Sate table? Give an Example	2M