17EC33

Visvesvaraya Technological University, Belagavi

MODEL QUESTION PAPER

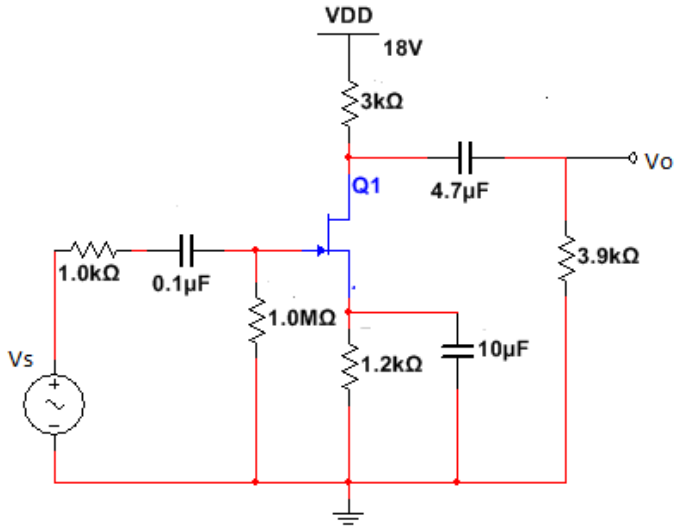
3rd Semester, B.E (CBCS 2017-18 Scheme)EC/TC

Course: 17EC33- Analog Electronics, *Set no. 1*

Time: 3 Hours **Max. Marks: 100**

Note: (i) Answer Five full questions selecting any one full question from each Module.
(ii) Question on a topic of a Module may appear in either its 1st or/and 2nd question.

		Module-1	Marks
1	a.	Obtain the expressions for Z_I, Z_O and A_V for the emitter follower configuration transistor circuit.	7
	b.	For the voltage divider bias circuit with, R_1=39KΩ, R_2=4.7KΩ, R_C=3.9KΩ and R_E = 1.2KΩ, find r_e, Z_i, Z_o and A_v. The values of β=100 and r_o=50KΩ.	7
	c	Draw and explain the hybrid-π model of transistor in CE configuration mentioning the significance of each component.	6
		OR	
2	a.	With the relevant expressions and circuits, obtain the re model for the common emitter transistor configuration.	6
	b.	Given I_E=2.5mA, h_{fe}=140, h_{0e}=20μS and h_{ob}=0.5μS. Obtain the common emitter hybrid equivalent circuit.	5
	c	Draw and explain the hybrid-π model of transistor in CE configuration mentioning the significance of each component.	5
	d	Draw the Darlington connection and explain its features.	4
		Module-2	
3	a.	With cross sectional view and transfer characteristics explain the working of Depletion type MOSFET.	7
	b.	Describe Shockley's equation for JFET. Obtain and plot the transfer characteristics for n channel JFET with I_{DSS} = 8mA and V_P = -5V.	6
	c	Derive an expression for output resistance and voltage gain of fixed bias FET amplifier	7
		OR	
4	a.	Explain the basic operation and characteristics of enhancement type MOSFET .	7
	b	Define transconductance of a JFET. Obtain the expression and show the dependency of transconductance with V_{GS} and I_D.	5
	c	The self bias configuration has V_{GS}=-2.6V, I_D=2.6mA, and I_{DSS}=8mA, V_P=-6V, y_{os}=20μS. Determine g_m, Z_i, Z_O and A_V with and without Cs.	8

		Module-3	
5	a.	Derive the expressions for low frequency cut-offs for a voltage divider transistor configuration with R_s and R_L.	8
	b.	For the circuit shown in Fig. Q5(b), with C_{Wi} = 3 pF, C_{Wo} = 5 pF, C_{gd} = 4 pF, C_{gs}= 6 pF, C_{ds} = 1 pF and I_{DSS}= 6 mA, V_P = -6V, r_d = ∞ Ω. i) Deterimeg$_m$and A_v ii) Determine f_{Hi} and f_{Ho} iii) Sketch the frequency response for the high frequency region using Bode plot and determine the cut-off frequency.  Fig.Q5(b)	12
		OR	
6	a.	What is Miller effect? Derive expression for Miller capacitance for an amplifier.	8
	b	For the circuit shown in Fig.6(b) with β=100 and r_0=40kΩ. i) Determine r_e and A_{vmid} ii) Calculate Z_i iii) Determine f_{Ls}, f_{Lc} and f_{LE} and determine the lower Cut-off frequency iv) Sketch the asymptotes of the Bode plot.	12

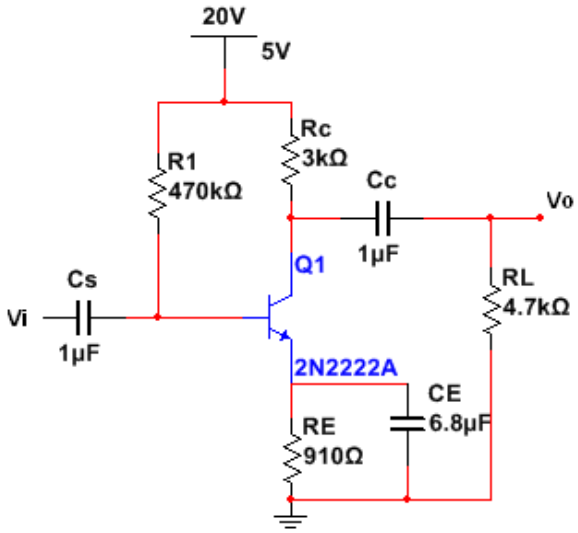


Fig.Q6(b)

		Module-4	12
7	a.	With a neat figure describe the voltage series feedback connection. Derive the expression for voltage gain, input impedance and output impedance.	7
	b.	With a neat circuit and necessary equations explain the working of Wien bridge oscillator	6
	c	With neat circuit diagram explain the working of series crystal oscillator. For a crystal which has L = 334mH, C = 0.065nF, C_M= 1pF, R = 5.5kΩ, calculate series resonant frequency of crystal oscillator.	7
		OR	
8	a.	Calculate the voltage gain of the current series feedback circuit shown in Fig.8(a) with h_{fe}=120, h_{ie}=900Ω.	7

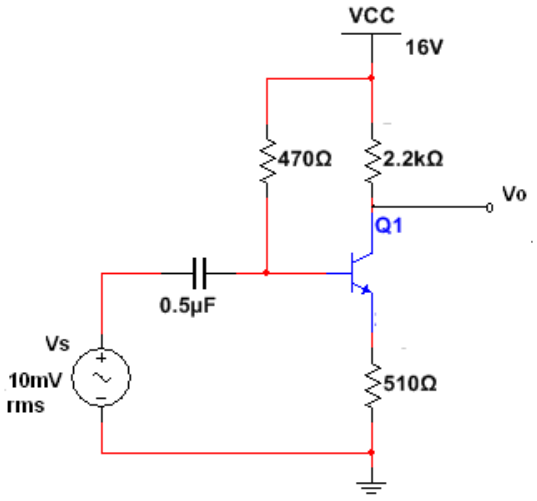


Fig.8(a)

	b.	With neat circuit diagram and necessary expressions, explain the working of practical FET phase shift oscillator.	6
	c.	With neat circuit diagram and waveform explain the working of UJT oscillator.	7
		Module-5	
9	a.	What is voltage regulator? With a neat circuit explain series voltage regulator using transistors.	8
	b.	What are the different types of power amplifiers? Show that The maximum conversion gain of transformer coupled class A amplifier is 50%.	7
	c	Calculate the harmonic distortion components for an output signal having fundamental amplitude of 2.5 V, second harmonic amplitude of 0.25 V, third harmonic amplitude of 0.1 V, and fourth harmonic amplitude of 0.05 V.	5
		OR	
10	a.	With a neat circuit diagram and waveforms derive an expression for conversion gain of Class B push pull amplifier.	8
	b	Derive the expression for second harmonic distortion.	6
	c	Draw the circuit diagram of a basic transistor shunt regulator and write the expression for output voltage. Determine the regulated voltage and circuit currents: I_Z, I_C and I_L if Rs=120Ω, RL=100Ω, V_Z=8.2V and V_i=22V.	6

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