17EC33

Visvesvaraya Technological University, Belagavi

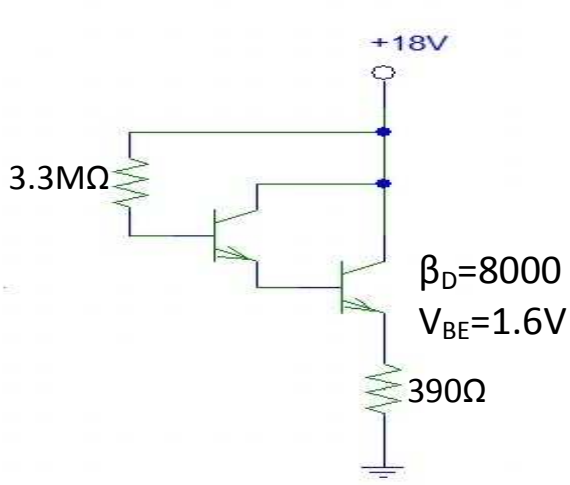
MODEL QUESTION PAPER

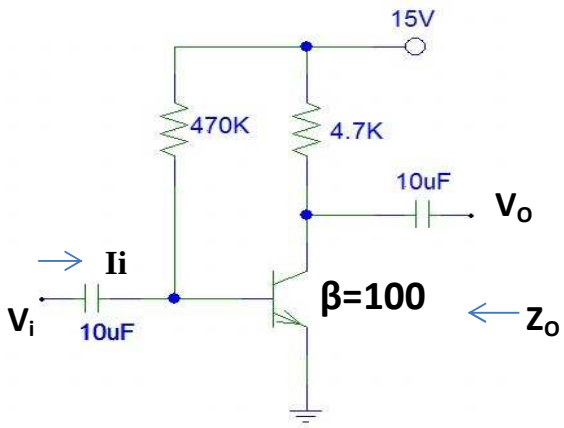
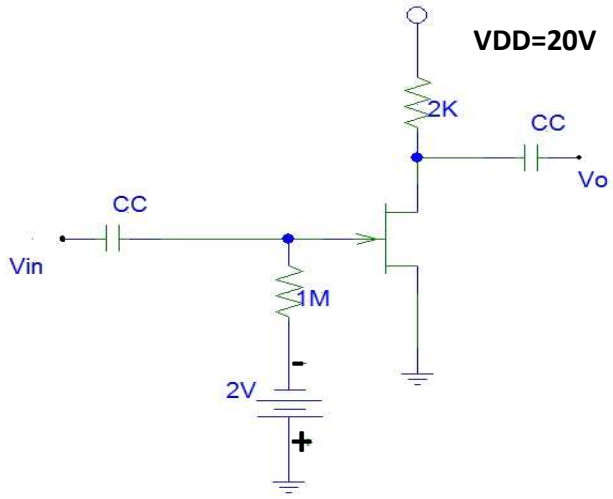
3rd Semester, B.E (CBCS 2017-18 Scheme) EC/TC

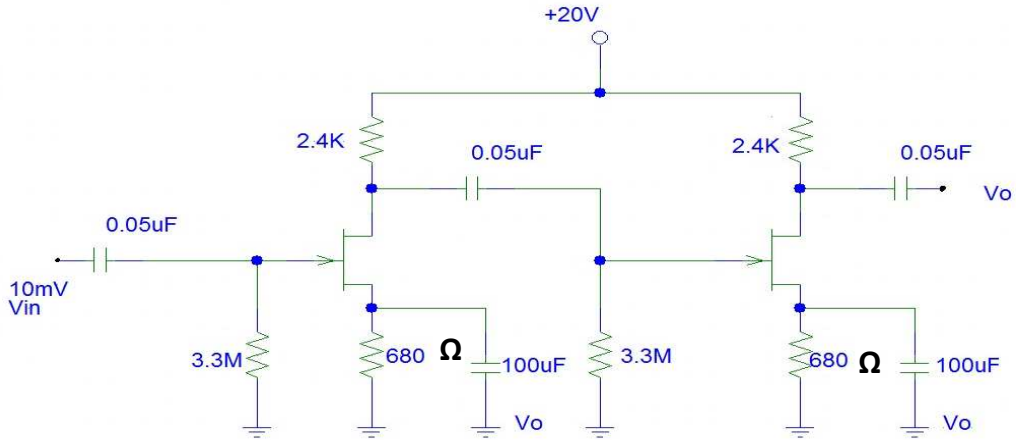
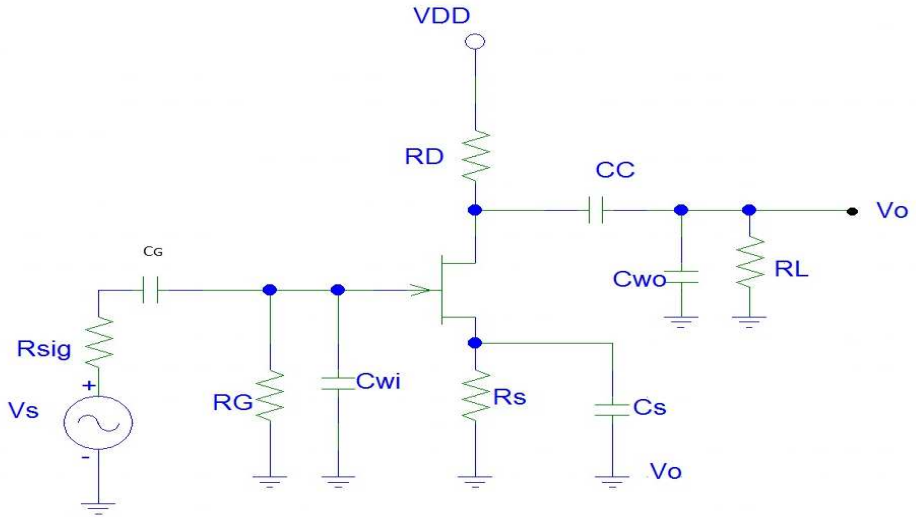
Course: 17EC33- Analog Electronics, *Set no. 2*

Time: 3 Hours **Max. Marks: 100**

Note: (i) AnswerFive full questions selecting any one full question from each Module.
(ii) Question on a topic of a Module may appear in either its 1st or/and 2nd question.

		Module-1	Marks
1	a)	Define h parameters and hence derive h parameters model of a CE BJT	5
	b)	Derive the expressions for A_I, A_V, Z_i and Z_O for a voltage divider bias circuit of BJT, Using re equivalent model of BJT. Show the phase relationship between input and output wave form.	10
	c)	What is Darlington Connection? Calculate the DC bias voltage and currents in the Darlington emitter follower circuit having V_{CC}=18V, R_E=390Ω, R_B=3.3MΩ, V_{BE}=1.6V β_D=8000  	5
		OR	
2	a)	Give the relation between re parameters and h parameters. What are the advantages of h parameters.	5
	b)	Derive the Expressions for current gain, voltage gain, input impendence and output impendence for anemitter follower circuit.	10

	c)	For the fixed bias network with V_{CC}=15V, R_B=470KΩ, R_C=4.7KΩ, C_{C1}=C_{C2}=10μF, β=100,r_0=50KΩ a) Determine re, Z_i,Z_O, A_V (with ro=∞Ω), Av with ro=50KΩ 	5
		Module-2	
3	a)	Explain the construction of N channel JFET. Also explain the drain and transfer characteristics of the JFET.	6
	b)	With Equivalent circuit obtain the expression for Z_O and A_V for JFET Self bias with unbypassed R_S.	8
	c)	The fixed bias configuration shown in has V_{GSQ}=-2V, I_{DQ}=5.625mAwith I_{DSS}=10mA,V_P=-8V and Yo_S=40μs, VGG = -2V, V_{DD}=20V,R_D=2KΩ, R_G=2MΩ. Determine gm, rd, Z_O and A_V 	6
		OR	
4	a)	Differentiate between Enhancement and Depletion MOSFET.	6
	b)	With necessary equivalent circuit obtain the expression for Z_i and A_V for a JFET Common Gate configuration.	8

	c)	Calculate the DC bias, overall voltage gain. For the cascaded identical common source amplifier with I_{DSS}=10mA V_P= -4V, VDD=20V, $R_{D1}=R_{D2}$=2.4KΩ, $R_{G1}=R_{G2}$=3.3MΩ, $R_{S1}=R_{S2}$=680Ω,$C_{S1}=C_{S2}$=100µF, $C_{C1}=C_{C2}=C_{C3}$=0.05µF. 	6
		Module-3	
5	a)	The input power to a device is 10000W at a voltage of 1000V. The output power is 500W and the output impedance is 20Ω. i) Find the power gain in decibels. ii) Find voltage gain in decibels.	5 10
	b)	Discuss the low frequency response of BJT amplifier and give expression for lower cutoff frequency due to C_C,C_E and C_S.	5
	c)	Calculate the overall lower 3db and upper 3db frequencies for a 3 stage amplifier having an individual f_1=40H_Z and f_2=2MH_Z	
		OR	
6	a)	Discuss the effect of various capacitors in frequency response of an amplifier.	5
	b)	Determine the high cutoff frequencies for the common source amplifier, C_G =0.01µF, C_C=0.5µF, C_S=2µF, R_{sig}=10KΩ, R_G=1MΩ ,R_D=4.7KΩ, R_S=1KΩ, R_L= 2.2KΩ I_{DSS}=8mA, V_P=-4V, rd=∞Ω , VDD=20V 	10
	c)	Describe miller effect and derive an equation for miller input capacitance.	5

		Module-4	
7	a)	With block diagram explain the concept of feedback amplifier.	5
	b)	Derive the expression for Z_{if} and Z_{of} voltage series feedback amplifier.	5
	c)	For a practical current series feedback circuit derive expression for A_F and $Z_{if.}$	10
		OR	
8	a)	What is an Oscillator? Discuss the concept of generating oscillations with the help of Barkhausen criteria.	5
	b)	Explain the operation of UJT Relaxation oscillator.	5
	c)	With a neat diagram and necessary expressions explain Hartley oscillator.	10
		Module-5	
9	a)	Give the definition of power amplifier and list the types of power amplifier based on the location of Q point.	5
	b)	Explain the working of class B. Push pull amplifier. Obtain an expression for maximum conversion efficiency of this amplifier.	10
	c)	Calculate the harmonic distortion components for an output signal having fundamental amplitude of 2.5V, Second harmonic amplitude of 0.25V, third harmonic amplitude of 0.1 V and fourth harmonic amplitude of 0.05 V and also calculate the total harmonic distortion for the amplitude components given above.	5
		OR	
10	a)	With necessary circuit diagram and characteristics curve, show that the maximum efficiency of a series fed class A amplifier is 25%.	10
	b)	Describe with block diagram the series and shunt type of voltage regulators.	5
	c)	Derive the voltage stability factor and output resistance for emitter follower series regulator.	5

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