15EC53

Visvesvaraya Technological University, Belagavi

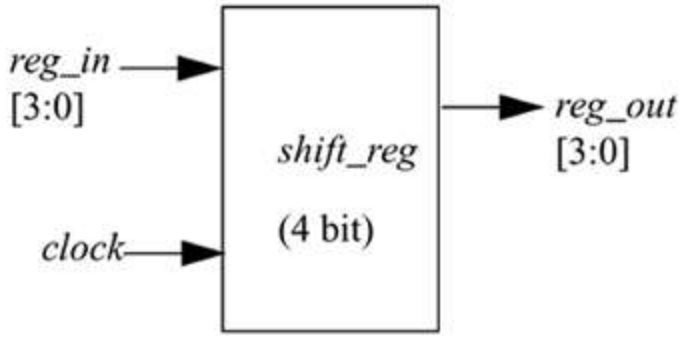
MODEL QUESTION PAPER

5th Semester, B.E (CBCS) EC

Course: 15EC53 - Verilog HDL

Note: (i) Answer Five full questions selecting any one full question from each Module.
(ii) Question on a topic of a Module may appear in either its 1st or 2nd question.

Time: 3 Hrs **Max. Marks: 80**

		Module-1	
1	a.	Explain a typical design flow for designing VLSI IC circuits using the block diagram.	08
	b.	Explain the different levels of Abstraction used for programming in Verilog.	08
		OR	
2	a.	Explain a top-down design methodology and a bottom-up design methodology.	10
	b.	Explain the factors that have made Verilog HDL popular.	06
		Module-2	
3	a.	Write a note on i) Comments ii) Number Specification iii) X and Z values and iv) Identifiers and Keywords with suitable examples.	10
	b.	Explain a Components of a Verilog Module with a neat block diagram.	06
		OR	
4	a.	Explain $display and $monitor tasks with examples.	10
	b.	A 4-bit parallel shift register has I/O pins as shown in the figure below. Write the module definition for this shift register. Include the list of ports and port declarations (no need to show the internals). 	06
		Module-3	
5	a.	Explain the instantiation of gates by writing a gate level module by name *gates* in Verilog.	04

	b.	Explain regular assignment delay in dataflow level of abstraction in Verilog.	04
	c.	The input output expressions for 1-bit Full Adder are given as sum= a ^ b^ c; co= (a &b)|(b&c)|(c&a). Write the gate level abstraction of 1-bit Full Adder by instantiating and, or, xor gates only.	08
		OR	
6	a.	Write the Verilog description of 4-bit Ripple carry Adder at Gate level Abstraction.	08
	b.	Write a program for 4-to-1 Multiplexer, Using Conditional Operators in dataflow level of abstraction in Verilog.	08
		Module-4	
7	a.	Explain combined port declaration and combined ANSI C style port declaration with examples in Verilog.	04
	b.	Explain the conditional statements in Verilog.	04
	c.	Write a behavioral 4 bit counter program in Verilog.	08
		OR	
8	a.	Explain different Loop statements in Verilog.	08
	b.	Write a Verilog behavioral 4 to 1 Multiplexer program using CASE statement.	08
		Module-5	
9	a.	Explain the synthesis process with a block diagram.	08
	b.	Write the VHDL entity declaration of 4- bit Ripple Carry Adder with the help of lock diagram of 4- bit Ripple Carry adder.	08
		OR	
10	a.	Explain the relationship between a design entity and its entity declaration and architecture body in VHDL.	08
	b.	Explain the declaration of constant, variable and signal in VHDL with examples.	08

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