15EC552

Visvesvaraya Technological University, Belagavi
MODEL QUESTION PAPER
5th Semester, B.E (CBCS) EC/TC

Course: 15EC552 - Switching & Finite Automata Theory

Note: (i) Answer Five full questions selecting any one full question from each Module.
(ii) Question on a topic of a Module may appear in either its 1st or 2nd question.

Time:3 Hrs **Max. Marks:80**

MODULE - 1			
1	a.	Explain the concept of Threshold Logic.	6
	b.	Discuss the following: (i) Elementary Properties (ii) Unate Function	6
	c.	Determine which of the functions is Unate. Show its minimal form. (i) $f(x_1, x_2, x_3, x_4) = \sum (1,2,3,8,9,10,11,12,14)$ (ii) $f(x_1, x_2, x_3, x_4) = \sum(2,3,6,10,11,12,14,15)$	4
OR			
2	a.	Given the switching function f(x1, x2, x3, x4) = ∑ (2, 3, 6, 7, 10, 12, 14, 15). Find a minimal threshold logic realization.	8
	b.	Show that threshold logic realization of Full Adder requires only two threshold elements.(Note that both sum and carry must be generated)	8
MODULE - 2			
3	a.	Use the map method to find a minimal set of tests for multiple faults for the two-level AND – OR realization of the function f(w, x, y, z) = wz' + xy' + w'x + wx'y	8
	b.	Explain the basic principle of one dimensional path sensitization method.	6
	c.	Define (i) Hazards (ii) Fault Table	2
OR			
4	a.	Discuss the following: (i) Possible strategies in Fault Tolerant Design (ii) Restoring Organs	8
	b.	List the properties of Boolean Differences.	4
	c.	Write a note on Preset Experiments.	4
MODULE - 3			

5	a.	Find the minimal form of machine M shown in Table Q.5(a). Also find the isomorphic machine and deduce its standard form. Table Q.5(a) PS | NS, Z: X=0, X=1 A: E,0 C,0 B: C,0 A,0 C: B,0 G,0 D: G,0 A,0 E: F,1 B,0 F: E,0 D,0 G: D,0 G,0	10
	b.	Define the following: (i) Synchronous Sequential Machine (ii) Equivalent States (iii) Compatible States (iv) Closed State & Closed Covering (v) Compatibility Graph (vi) Merger Table	6
		OR	
6	a.	What is Merger Graph? Draw the Merger Graph and corresponding compatibility graph for the incompletely specified machine M shown in Table Q.6(a). Table Q.6(a) PS | NS, Z: I1, I2, I3, I4 A: - C,1 E,1 B,1 B: E,0 - - - C: F,0 F,1 - - D: - - B,1 - E: - F,0 A,0 D,1 F: C,0 - B,0 C,1	10
	b.	Explain the concept of state equivalence	6
		MODULE - 4	
7	a.	Explain input independence and autonomous clock. For the Machine M shown in Table Q.7(a) find input consistent partition. If the assignments are as follows, find the logical equation for the machine. **Assignments** : A – 000, B - 001, C - 010, D - 011, E - 100, F -101 Draw the realization of machine M using autonomous clock and draw the autonomous clock of machine M. Table Q.7(a) **PS** | **NS**: **X=0**, **X=1** | **Z**: **X=0**, **X=1** A: D C 0 1 B: C D 0 0	10

			C	E	F	0	1	
			D	F	F	0	0	
			E	B	A	0	1	
			F	A	B	0	0	
	b.	What are Covers and implication graph? Explain						6
OR								
8	a.	For the machine M shown in Table Q.8(a), give the closed partition by state splitting. Write the corresponding logical equation and implication graph.						8
		Table Q.8(a)						
			PS	NS		Z		
						X=0	X=1	
				X=0	X=1			
			A	A	B	0	1	
			B	C	B	0	0	
			C	A	C	0	0	
	b.	Write an explanatory note on Parallel Decomposition						8
MODULE - 5								
9	a.	What is an experiment? Explain types of experiments with reference to fault detection.						6
	b.	Describe the concept of Machine Identification.						6
	c.	Write a note on diagnosable machines						4
OR								
10.	a.	Explain Second algorithm for the design of fault detection experiments						6
	b.	Prove the theorem : If an n-state machine has a synchronizing or sequences, then it has one such sequences whose length is at most n(n+1)(n-1) / 6						10