6th Semester BE (CBCS) EC/TC Model Question Papers

15EC61

Visvesvaraya Technological University, Belagavi

MODEL QUESTION PAPER

6th Semester, B.E (CBCS) EC/TC

Course: 15EC61 - Digital Communication

Max Marks: 80 **Time: 3 Hours**

Note: (i) Answer Five full questions selecting any one full question from each Module.

(ii) Question on a topic of a Module may appear in either its 1st or/and 2nd question.

Module 1			
1	(a)	Define Hilbert Transform. State the properties of it.	4
	(b)	Define the complex envelope of bandpass signals. Obtain the canonical representation of bandpass signals	6
	(c)	Derive the power spectral density of polar NRZ signals and plot the spectrum.	6
OR			
2	(a)	Define the Pre-envelope. Show the spectral representations of pre-envelopes for low pass signals.	4
	(b)	Derive the expression for the complex low pass representation of bandpass systems.	7
	(c)	Given the data stream 1110010100. Sketch the transmitted sequence of pulses for each of the following line code. (i) Unipolar NRZ (ii) Polar NRZ (iii) Unipolar RZ (iv) bipolar RZ (v) Manchester code.	5
Module 2			
3	(a)	Explain the Geometric representation of signals and express the energy of the signal in terms of the signal vector.	5
	(b)	Explain the Gram-Schmidt orthogonalization procedure.	5
	(c)	Explain the matched filter receiver with the relevant mathematical theory.	6
OR			
4	(a)	Obtain the decision rule for Maximum likelihood decoding and explain the correlation receiver.	7
	(b)	The waveforms of four signals $s_1(t)$, $s_2(t)$, $s_3(t)$, and $s_4(t)$ described below. $s_1(t) = 1, \quad 0 < t < T/3,$ $s_2(t) = 1, \quad 0 < t < 2T/3,$ $s_3(t) = 1, \quad T/3 < t < T,$	9

		$s_4(t) = 1, \quad 0 < t < T$, and zero otherwise. Using the Gram-Schmidt orthogonalization procedure, find an orthonormal basis for this set of signals and construct the corresponding signal-space diagram.	
Module 3			
5	(a)	Define binary phase shift keying. Derive the probability of error of BPSK.	7
	(b)	Define M-ary QAM. Obtain the constellation of QAM for M=4 and draw the signal space diagram	4
	(c)	Given the input binary sequence 1100100001. Sketch the waveforms of the inphase and quadrature components of a modulated wave and next sketch the QPSK signal.	5
OR			
6	(a)	Describe the QPSK signal with its signal space characterization. With a neat block diagram explain the generation and detection of QPSK signals.	6
	(b)	Obtain the expression probability of symbol error of coherent binary FSK.	7
	(c)	Illustrate the operation of DPSK for the binary sequence 10010011	3
Module 4			
7	(a)	With a neat block diagram Explain the digital PAM transmission through bandlimited baseband channels and obtain the expression for ISI.	5
	(b)	What are adaptive equalizers? Explain the linear adaptive equalizer based on the MSE criterion.	6
	(c)	The binary sequence 10010110010 is the input to the precoder whose output is used to modulate a duobinary transmitting filter. Obtain the precoded sequence, transmitted amplitude levels, the received signal levels and the decoded sequence.	5
OR			
8	(a)	What is eye pattern? What is the Nyquist criterion for zero ISI? Given an example of the pulse with zero ISI.	5
	(b)	Explain the design of bandlimited signals with controlled ISI. Describe the time domain and frequency domain characteristics of a duobinary signal.	5
	(c)	What is channel equalization? With a neat diagram explain the concept of equalization using a linear transversal filter.	6
Module 5			
9	(a)	Draw the 4 stage linear feedback shift register with 1^{st} and 4^{th} stage is connected to Modulo-2 adder. Output of Modulo-2 is connected to 1^{st} stage input. Find the output PN sequence and obtain the autocorrelation sequence.	6
	(b)	With a neat block diagram explain the frequency hopped spread spectrum.	7
	(c)	Explain the effect of dispreading on narrowband interference.	3
OR			
10	(a)	Explain the generation of direct sequence spread spectrum signal with the relevant waveforms and spectrums.	6
	(b)	With a neat block diagram explain the CDMA system based on IS-95.	7
	(c)	Write a short note on application of spread spectrum in wireless LANs.	3

Visvesvaraya Technological University, Belagavi
MODEL QUESTION PAPER – Set I
VI Semester, B.E (CBCS) EC/TC

Course: 15EC62 - ARM Microcontroller and Embedded Systems

Note: (i) Answer Five full questions selecting any one full question from each Module.

(ii) Question on a topic of a Module may appear in either its 1st or/and 2nd question.

Time: 3 hrs **Max. Marks: 80**

MODULE – 1			
1	a	Briefly describe the functions of the various units with the architectural block diagram of ARM Cortex M3.	6
	b	Explain the applications of Cortex M3.	3
	c	Discuss the functions of R0 to R15 and other special registers in Cortex M3.	7
OR			
2	a	Describe the functions of exceptions with a vector table and priorities.	6
	b	Explain the operation modes of Cortex M3 with diagrams.	3
	c	Explain two stack model and reset sequence in ARM cortex M3.	7
MODULE -2			
3	a	Explain the following 16 bit instructions in Cortex M3: ADC, RSB, TST, BL, LDR, MOV, SVC, PUSH	7
	b	Write an ALP to find the sum of first 10 integer numbers.	4
	c	Write the memory map of Cortex M3 and explain briefly bit-band operations.	5
OR			
4	a	Explain the following 32 bit instructions in Cortex M3: AND, CMN, MLA, SDIV, STR, MRS, MRS, POP	8
	b	Write a C language program to toggle an LED with a small delay in Cortex M3.	4
	c	With a diagram, explain the organization of CMSIS.	4
MODULE - 3			
5	a	Explain the 6 purposes of Embedded systems with an example for each.	6
	b	Differentiate between (i) General Computing Systems and Embedded Systems and (ii) RISC and CISC architectures	4
	c	Explain the 3 classifications of Embedded systems based on complexity and performance.	3
	d	Mention the applications of Embedded systems with an example for each.	3
OR			
6	a	Explain the functions of Optocoupler and SPI bus with diagrams.	6
	b	Write a note on Embedded firmware.	4
	c	Explain SRAM design and features with a diagram.	3

	d	Write the architectural block diagram of embedded system and mention the components used.	3
MODULE – 4			
7	a	Explain the 6 operational quality attributes of an embedded systems.	5
	b	Define the 6 characteristics of an embedded system.	5
	c	With a block diagram, mention the components used in the design of a washing machine and also explain its working.	6
OR			
8	a	Compare DFG and CDFG with an example and diagrams.	4
	b	With FSM model, explain the design and operation of automatic tea/coffee vending machine.	5
	c	Explain the assembly language based embedded firmware development with a diagram and mention its advantages and disadvantages.	7
MODULE – 5			
9	a	Briefly explain the functions of the operating system, with a diagram.	4
	b	Describe preemptive SJF scheduling. Determine average turn around time and average waiting time, if processes P1 P2 and P3 with estimated completion time of 10, 5, 7 milliseconds enter ready queue together and later P4 with a completion time of 2 msec enters ready queue after 2 msec.	5
	c	With a state transition diagram, structure and memory organization of a process, describe the process state transitions.	7
OR			
10	a	Explain out of circuit and in-system programming methods for integration of hardware and firmware.	5
	b	With a diagram, mention the function of the components in an embedded system development environment.	5
	c	Explain simulator based debugging and ICE based target debugging techniques.	6

Note: In the updated syllabus 'Bus Interface' topic in Module-2 has been replaced with 'Bit-band operations.

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15EC62

Visvesvaraya Technological University, Belagavi

MODEL QUESTION PAPER – Set II

6th Semester, B.E (CBCS) ECE

Course: 15EC62- ARM Microcontroller and Embedded Systems

Time: 3 Hours **Max. Marks: 80**

Note: (i) Answer Five full questions selecting any one full question from each Module.
(ii) Question on a topic of a Module may appear in either its 1st or/and 2nd question.

		Module-1	**Marks**
1	a	Explain the architecture of ARM Cortex-M3 processor with the help of a neat block diagram.	10M
	b	List the applications of ARM Cortex-M3 processor.	06M
		OR	
2	a	Explain ARM Cortex-M3 Program Status Register in detail.	08M
	b	Explain Stack PUSH and POP operation in Cortex-M3 with the help of a neat diagram.	04M
	c	Explain reset sequence with the help of memory map.	04M
		Module-2	
3	a	Explain the following instructions with example i)ASR ii)LSL iii)ROR iv)REV	08M
	b	List and explain the function of any four data processing and branch instructions in Cortex- M3 with example.	08M
		OR	
4	a	Write a note on the interface between assembly and C.	04M
	b	Explain any two methods of accessing memory mapped registers in C.	08M
	c	List and explain the function of any four commonly used memory access instructions in Cortex- M3	04M
		Module-3	
5	a	Explain the components of typical Embedded Systems in detail.	08M
	b	Give the memory classification. Explain the SRAM cell implementation with relevant	

		figures.	08M
		OR	
6	a	Explain the different on-board communication interfaces in brief.	08M
	b	Differentiate between computer system and an Embedded System.	08M
		Module-4	
7	a	Explain the different characteristics of Embedded System in detail.	08M
	b	What is operational quality attribute? Explain the important non- operational quality attributes to be considered in any Embedded System design.	08M
		OR	
8	a	Explain the different Embedded firmware design approaches in detail.	08M
	b	What is Hardware and Software co-design? Explain the fundamental design approaches in detail.	08M
		Module-5	
9	a	Explain Multi processing, multi tasking and multi programming.	08M
	b	What the basic functions of real time kernel? Explain each	08M
		OR	
10	a	Explain the Simulator and Emulator.	08M
	b	Explain the terms process, task and thread	08M

Note: In the updated syllabus 'Bus Interface' topic in Module-2 has been replaced with 'Bit-band operations'.

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15EC63

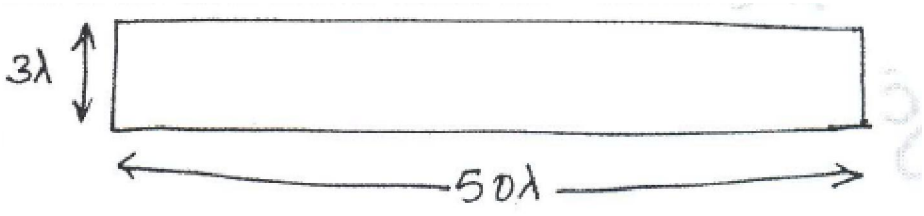
Visvesvaraya Technological University, Belagavi
MODEL QUESTION PAPER- Set I
6th Semester, B.E (CBCS) ECE

Course: 15EC63- VLSI DESIGN

Time: 3 Hours **Max. Marks: 80**

Note: (i) Answer five full questions selecting any one full question from each Module.

(ii) Question on a topic of a Module may appear in either its 1st or/and 2nd question.

		Module-1	**Marks**
1	a	What do you mean by static load inverters? Derive the output voltage for pseudo Inverter by discussing its dc characteristics.	8
	b	Derive the CMOS inverter DC characteristics graphically from p device and n device characteristics and show all operating regions.	8
		OR	
2	a	Explain the nMOS enhancement mode transistor operation for different values of V_{gs} and V_{ds} .	6
	b	Explain the fabrication steps of CMOS p-well process with neat diagram and write the mask sequence.	6
	c	What are the advantages of BiCMOS process over CMOS technology.	4
		Module-2	
3	a	Explain λ based design rules with neat diagram.	6
	b	Draw the circuit and stick diagram for nMOS and CMOS implementation of Boolean expression = +	10
		OR	
4	a	Calculate the capacitance in □C_g for the given metal layer shown in the Fig Q4(a), if feature size=5µm and relative value of metal to substrate =0.075.  **Fig Q4(a)**	8
	b	Define sheet resistance R_s and standard unit of capacitance (□C_g). Calculate the on resistance of 4:1 nMOS inverter with R_s=10kΩ/□, Z_{pu}=8λ/2λ, Z_{pd}=2λ/2λ. Also	8

		estimate the total power dissipated if V_{DD}=5V.	
Module-3			
5	a	Find the scaling factors for: i) Saturation current ii) Current density iii) Power dissipation/unit area iv) Maximum operating frequency	8
	b	Design a 4 bit ALU to implement addition, subtraction, EX-OR, EX-NOR, OR and AND operations.	8
OR			
6	a	With a neat diagram, explain 4x4 barrel shifter.	8
	b	Describe Manchester Carry-chain.	8
Module-4			
7	a	Discuss the architectural issues related to subsystem.	8
	b	Explain Pseudo nMOS logic for NAND gate and Inverter.	8
OR			
8	a	Explain Parity generator with basic block diagram and stick diagram.	8
	b	Explain FPGA architectures.	8
Module-5			
9	a	Explain 3 transistor dynamic RAM cell.	8
	b	Write a note on testability and testing.	8
OR			
10	a	Explain the scan design techniques.	8
	b	Demonstrate write operation & read operation for four transistor dynamic and six transistor static CMOS memory cell.	8

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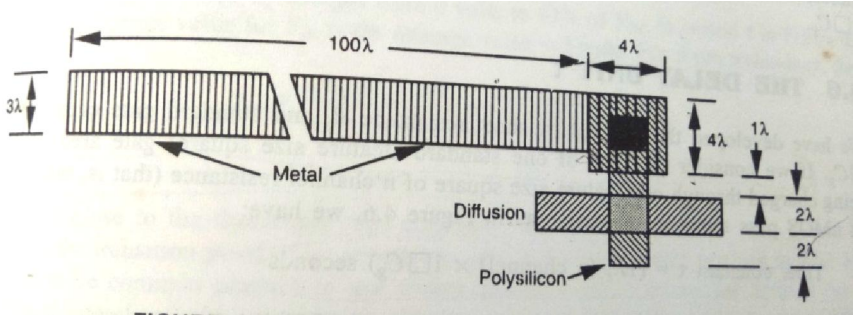
15EC63

Visvesvaraya Technological University, Belagavi
MODEL QUESTION PAPER –Set II
6th Semester, B.E (CBCS) EC

Course: 15EC63- VLSI DESIGN

Time: 3 Hours **Max. Marks: 80**

Note: (i) Answer Five full questions selecting any one full question from each Module.
(ii) Question on a topic of a Module may appear in either its 1st or/and 2nd question.

		Module-1	Marks
1	(a)	With Suitable diagrams explain the three regions of operation of Enhancement mode NMOS transistor.	7
	(b)	Using graphical approach explain the DC characteristics of a CMOS inverter.	5
	(c)	Differentiate between CMOS and Bipolar technologies.	4
		OR	
2	(a)	With neat sketches explain the CMOS P-well process steps to fabricate a CMOS inverter.	6
	(b)	Derive a first order expression relating the current and voltage (I-V) for an NMOS transistor in Linear region.	6
	(c)	Explain only two non ideal I-V effects in a MOS device.	4
		Module-2	
3	(a)	What do you mean by λ-based design rules? List the λ-based design rules for CMOS Technology.	7
	(b)	Draw the schematic, stick diagram and layout for a CMOS NAND gate.	9
		OR	
4	(a)	Derive the expression for sheet resistance Rs.	4
	(b)	Calculate the capacitance of the structure given below in Figure 4(b)  **Figure 4(b)**	6
	(c)	Derive an expression for the estimation of CMOS inverter Delay.	6
		Module-3	

5	**(a)**	Obtain the scaling factor for the following device parameters: (I) Gate Capacitance (II) Gate Area (III) Saturation Current (Idss) (IV) Channel Resistance (Ron) (V) Max Operating Frequency (fo) (VI) Power Dissipation per gate (Pg) (VII) Current density (J)	**8**
	(b)	(VIII) Gate delay (Td). With a neat diagram explain 4x4 Barrel shifter.	**8**
		OR	
6	**(a)**	Explain the general arrangement of a 4 bit ALU.	**8**
	(b)	Explain in detail any One Adder Enhancement technique.	**8**
		Module-4	
7	**(a)**	Discuss the architectural issues to be followed in the design of a VLSI subsystem.	**5**
	(b)	Explain in detail the Generic Structure of an FPGA fabric.	**7**
	(c)	Explain switch logic implementation of a 4x4 four way multiplexer.	**4**
		OR	
8	**(a)**	Explain the Structured Design approach for the implementation of a Parity Generator with	**8**
	(b)	relevant stick diagram. Explain Dynamic CMOS logic with an example.	**8**
		Module-5	
9	**(a)**	Explain 3-Transistor Dynamic RAM cell with Schematic and stick diagram.	**6**
	(b)		**4**
	(c)	List the System timing Considerations. Explain any two fault models in combinational circuits.	**6**
		OR	
10	**(a)**	Explain Pseudo-Static RAM cell (CMOS) with schematic and stick diagram.	**8**
	(b)	Write short notes on I) Observability and Controllability II) Built in Self Test (BIST)	**8**

15EC64

Visvesvaraya Technological University, Belagavi
MODEL QUESTION PAPER – Set I
6th Semester, B.E (CBCS) EC/TC

Course: 15EC64– Computer Communication Networks

Time: 3 Hours **Max Marks: 80**

Note: (i) Answer Five full questions selecting any one full question from each Module.
(ii) Question on a topic of a Module may appear in either its 1st or 2nd question.

Module 1			
1	(a)	Explain the significance of all layers in TCP/IP protocol suite	8
	(b)	Distinguish Character stuffing and Bit stuffing, with an example	4
	(c)	Explain four Physical Topologies.	4
OR			
2	(a)	Discuss the FSM for stop and wait protocol in detail using suitable example	8
	(b)	Write the format of an ARP packet, and show how ARP sends request and response message with suitable example	8
Module 2			
3	(a)	Discuss the behavior of the three persistence methods of CSMA with flow diagram	8
	(b)	Explain token passing as a controlled aces technique	4
	(c)	A slotted ALOHA network transmits 200 bit frame on a shared channel of 200 kbps. What is the throughput if the system (all stations together) produces	4

		(i)1000 frames per second (ii) 500 frames per second (iii)250 frames per second	
OR			
4	(a)	Explain the IEEE frame format of standard Ethernet	6
	(b)	Explain the standard Ethernet physical layer implementation of (i)10base 2 (ii)10base5	4
	(c)	With a neat diagram, explain Gigabit Ethernet encoding scheme.	6
Module 3			
5	(a)	Discuss the characteristics of wireless LAN protocol.	4
	(b)	Describe the characteristics of VLAN used to group stations and explain them briefly	6
	(c)	Explain spanning tree algorithm with graphical representation	6
OR			
6	(a)	Explain the two different approaches of Packet-switched network to route the packet.	8
	(b)	An organization is granted a block of addresses with the beginning address 14.24.74.0/24. The organization needs to have 3 subblocks of addresses to use in its three subnets: one subblock of 10 addresses, one subblock of 60 addresses, and one subblock of 120 addresses. Design the subblocks.	8
Module 4			
7	(a)	Explain IPv4 datagram format.	8
	(b)	Explain three phases of Remote host and Mobile host communication	8
OR			

8	(a)	Explain the operation of External and Internal Border Gateway Protocol	8
	(b)	Explain Least cost tree using shared link state database with suitable example	8
Module 5			
9	(a)	Explain connectionless and connection-oriented service represented as FSMs for transport layer	8
	(b)	Write outline and explain send window and receive window for selective repeat protocol	8
OR			
10	(a)	What are the different TCP services and features? Explain them	8
	(b)	Explain TCP connection establishment and connection termination using three way handshaking	8

Note: In the updated syllabus, in Module-3, Routers has been added along with the Switches.

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15EC64

Visvesvaraya Technological University, Belagavi

MODEL QUESTION PAPER – Set II

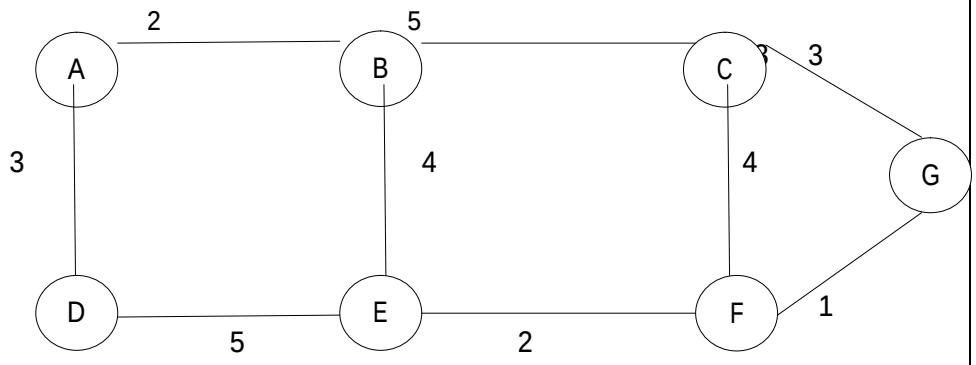
6th Semester, B.E (CBCS) EC/TC

Course: 15EC64- Computer Communication Networks

Time: 3 Hours **Max. Marks: 80**

Note: (i) Answer Five full questions selecting any one full question from each Module.
(ii) Question on a topic of a Module may appear in either its 1st or/and 2nd question.

		Module-1	Marks
1	a	Explain with neat diagrams the basic topologies for a network	06
	b	Explain with neat diagram the logical connection between layers and its function of TCP/IP Protocol suits.	05
	c	Illustrate with an example two types of framing	05
		OR	
2	a	Explain circuit switched and packet switched network	05
	b	Compare OSI with TCP/IP	06
	c	Explain ARP operation	05
		Module-2	
3	a	With neat diagrams , Explain persistence methods in CSMA	06
	b	With neat diagram , Explain Ethernet frame format .	05
	c	A pure ALOHA network transmits 200 bit Frames on a shared channel of 200kbps. What is the throughput if system produces : (i) 1000 Frames per sec (ii) 250 Frames per sec	05
		OR	
4	a	Describe polling and Token passing in controlled Access method	06
	b	Write short notes on 10 Base5 thick Ethernet, 10 Base 2 thin Ethernet	05
	c	A slotted ALOHA Network transmits 200bit Frames using a shared channel with a 200kbps bandwidth. Find the throughput if the system produces: (i) 1000 Frames per sec (ii) 250 Frames per sec	05
		Module-3	
5	a	Explain with architecture of two kinds of services in wireless Ethernet	06
	b	Apply spanning tree algorithm and mark forwarding and blocking ports for a system with 4 LANS and 5 switches. (i) S1 connects LAN1 and LAN2 (ii) S2 connects LAN1 and LAN3 (iii) S3 connects LAN2, LAN3 and LAN4 (iv) S4 connects LAN2, LAN4 (v) S5 connects LAN3, LAN4	06
	c	Explain Network Address Translation (NAT)	04

		OR	
6	a	With a neat diagram explain two types of Network defined by Bluetooth	06
	b	Explain VLAN with a neat diagram and also membership and configuration of VLAN	06
	c	Explain Forwarding process of a router	04
		Module-4	
7	a	With a neat diagram explain IPV4 Datagram format	06
	b	Explain with neat diagram the three phases in Mobile host communication	06
	c	With a neat diagram Describe areas in an Autonomous system in OSPF	04
		OR	
8	a	With a neat diagram explain general format of ICMP messages	06
	b	Apply link state routing for the given Fig. Q.8(b) below and create a least cost tree using Dijkstra Algorithm  Fig. Q. 8(b)	10
		Module-5	
9	a	Explain why the send window size for Go- Back N must be less than 2^m	05
	b	Explain sending and receiving buffers in TCP	05
	c	With a neat diagram explain TCP segment format	06
		OR	
10	a	Explain why the size of the send and receiver window in selective repeat can be atmost one half of 2^m	05
	b	Discuss the general services provided by UDP	05
	c	Explain with a neat diagram connection establishment using three way handshaking in TCP	06

Note: In the updated syllabus, in Module-3, Routers has been added along with the Switches.

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15EC651

Visvesvaraya Technological University, Belagavi

MODEL QUESTION PAPER

6th Semester, B.E (CBCS) EC/TC

Course: 15EC651 – Cellular Mobile Communications

Time: 3 Hours **Max. Marks: 80**

Note: (i) Answer Five full questions selecting any one full question from each Module.
(ii) Question on a topic of a Module may appear in either its 1st or/and 2nd question.

		Module-1	Marks
1	a)	What are co-channel cells? with a diagram & relevant equations, explain the interference between signals from co-channel cells.	8
	b)	Explain how cell splitting is used to improve coverage and capacity in cellular systems with a diagram.	8
		OR	
2	a)	Explain the three basic propagation mechanisms which impact propagation in a mobile communication system.	8
	b)	Explain okumura and hata outdoor propagation models.	8
		Module-2	
3	a)	Explain the impulse response model of a multipath channel with relevant equations.	8
	b)	Explain the clarke's model for flat fading with relevant equations.	8
		OR	
4	a)	Consider a transmitter which radiates a sinusoidal carrier frequency of 1850 MHz. For a vehicle moving 60mph, compute the received carrier frequency if the mobile is moving a) Directly towards the transmitter b) Directly away from the transmitter c) In a direction which is perpendicular to the direction of arrival of the transmitted signal.	6
	b)	What is small scale fading? explain different types of small-scale fading.	10
		Module-3	
5	a)	What is multiframe in GSM? explain the channel organization in a 51-frame multiframe.	8
	b)	With a simplified block diagram, explain the GSM speech coder.	8
		OR	
6	a)	Explain the GSM system architecture with a diagram.	8
	b)	Explain the GSM protocol architecture for signaling with a diagram.	
		Module-4	
7	a)	Explain the GPRS system architecture & interfaces with a diagram	8

	b)	Explain the location updating procedure used in GSM.	8
		OR	
8	a)	Explain the Multimedia messaging service network architecture (MMSNA) with a diagram.	8
	b)	Explain the effects of EDGE on the GSM system architecture	8
		Module-5	
9	a)	Explain the generation of the CDMA forward traffic/power control channel for 9.6 kbps	8
	b)	Explain the various states involved in CDMA call establishment	8
		OR	
10	a)	Explain the different types of CDMA handoff with neat diagrams.	8
	b)	Explain the evolution of CDMA to 3G with a diagram	8

15EC652

Visvesvaraya Technological University, Belagavi
MODEL QUESTION PAPER
6th Semester, B.E (CBCS) EC/TC

Course: 15EC652 - ADAPTIVE SIGNAL PROCESSING

Time: 3 Hours **Max. Marks: 80**

Note: (i) Answer Five full questions selecting any one full question from each Module.
(ii) Question on a topic of a Module may appear in either its 1st or/and 2nd question.

		Module-1	Marks
1	a.	Explain the characteristics and applications of adaptive signal processing.	8
	b.	With a neat diagram explain open and closed loop adaptation.	8
		OR	
2	a.	Discuss about Principle of Orthogonality.	8
	b.	Derive augmented Wiener-Hopf equation for forward prediction.	8
		Module-2	
3	a.	Explain about Gradient Search methods.	5
	b.	Discuss about Stability and Rate of convergence Gradient Searching Algorithm	7
		OR	
4	a.	Compare Newton's & Steepest-descent methods in terms of speed adaptation and mis-adjustment.	10
	b.	Discuss about role of Learning curves.	6
		Module-3	
5	a.	Derive LMS adaptive algorithm.	8
	b.	Compare the LMS and the RLS algorithm	8
		OR	
6	a.	Determine the response of the system given by $y(n)=2.5y(n-1)-y(n-2)+x(n)-5x(n-1)+6x(n-1)$ to a input ( )	6
	b.	Prove Correlation properties of lattice Filter.	10
		Module-4	
7	a.	Discuss the working of spread spectrum communication system.	8
	b.	Explain how adaptive filters can be used for single input system identification	8
		OR	
8	a.	Illustrate how adaptive filters are used to measure earth's impulse response.	10
	b.	Express the relevance of the term spread spectrum when information is represented by pseudo random sequence.	6
		Module-5	
9	a.	Describe the two types of inverse modelling approaches.	8
	b.	Derive the least-square solution to inverse modelling problem.	8
		OR	
10	a.	Discuss about Cancellation of Echoes in long distance telephone circuits.	10
	b.	Explain how poles and zeros can be adapted for IIR filter synthesis.	6

15EC653

Visvesvaraya Technological University, Belagavi

MODEL QUESTION PAPER

6th Semester, B.E (CBCS) EC/TC

Course: 15EC653 - ARITIFICAL NEURAL NETWORKS

Time: 3 Hours **Max. Marks: 80**

Note: (i) Answer Five full questions selecting any one full question from each Module.
(ii) Question on a topic of a Module may appear in either its 1st or/and 2nd question.

		Module-1	**Marks**
1	a.	What is Neural Learning? Draw and explain the general neuron model.	8
	b.	State and explain the Ex-OR problem? Also, explain how to overcome it.	8
		OR	
2	a.	List and explain any three commonly used activation functions in ANN?	8
	b.	Draw and explain architectural graph of a multi-layer perceptron with two hidden layers.	8
		Module-2	
3	a.	What is termination criterial in perceptron training, if the given samples are not linearly separable?	6
	b.	Discuss about Stability and Rate of convergence LMS Algorithm.	10
		OR	
4	a.	What is Back propagation? Explain the Back propagation-training algorithm with the help of a one hidden layer feed forward Network	10
	b.	Illustrate how LMS algorithm is used for noise cancellation	6
		Module-3	
5	a.	Derive LMS adaptive algorithm.	8
	b.	Compare RBF with Multilayer Perceptron.	8
		OR	
6	a.	Describe how RBB networks uses cover's theorem to solve complex classification problem.	8
	b.	Define the problem of automated face recognition system and its ANN solution.	8
		Module-4	
7	a.	What is the architecture of Hopfield network? Explain the working principal of Hopfield network with example	8
	b.	Explain how BAM can be used as Hetro-associative memory.	8
		OR	
8	a.	Explain how an unsupervised learning mechanism can be adopted to solve supervised learning task using LVQ algorithm.	10
	b.	Explain the concept of Simulated annealing.	6
		Module-5	
9	a.	Explain the concept of dimensionality reduction using principal component analysis.	8

	b.	Discuss any two applications of SOM.	8
		OR	
10	a.	Describe Kohonen self-organization map in detail.	10
	b.	Write a short note on Growing neural GAS algorithm.	6

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MODEL QUESTION PAPER – Set I

6th Semester, B.E (CBCS) EC/TC

Course: 15EC654-Digital Switching System

Time: 3 Hours **Max. Marks: 80**

Note: (i) Answer Five full questions selecting any one full question from each Module.
(ii) Question on a topic of a Module may appear in either its 1st or/and 2nd question.

		Module-1	Marks
1	a.	Explain in brief the operation of a four wire circuit used in two way transmission.	10
	b.	Explain in brief regulations, standards in a telecommunication network	6
		OR	
2	a.	Explain in brief PCM primary multiplex group.	8
	b.	Define the terms dB, dBW and dBm.	3
	c.	An amplifier has an input resistance of 600Ω and a resistive load of 75 Ω. When it has an r.m.s input voltage if 100mV, the r.m.s output current is 20mA. Find the gain in dB.	5
		Module-2	
3	a.	List out the difference between Message and circuit switching	6
	b.	What is the significance of distribution frames? Explain the operation of distribution frames.	10
		OR	
4	a.	What are the functions of Switching System?	8
	b.	Explain the basic call processing in DSS.	8
		Module-3	
5	a.	Derive the Erlang's second distribution equation in case of switching systems for a finite queue capacity.	10
	b.	During the busy hour a group of trunks is offered 100 calls having an average duration of 3 min; one call fails to find a disengaged trunk. Find the traffic offered to the group and the traffic carried by the group.	6
		OR	
6	a.	Find the grade of service when a total of 30E is offered to the 2 stage switching network and the traffic evenly distributed over the 10 outgoing routes. Also find traffic capacity if $B \leq 0.01$.	6

	b.	Define: a) GOS b) Busy hour c) CCR d) BHCA	4
	c.	Design a 3 stage fully interconnected network for 600 incoming trunks and 100 outgoing trunks that will make use of switches of size 5 x 5. Determine the number of cross points required.	6
		Module-4	
7	a.	An S-T-S network has 10 incoming and 10 outgoing highways. Each of which conveys 32 PCM channels between incoming and outgoing space switches; there are 20 lines containing time switches. During the busy hour, the network is offered 200E of traffic and it can be assumed that this is evenly distributed over the outgoing channel. Estimate the grade of service obtained if, i) Connection is required to a particular free channel on a selected outgoing highway (mode 1) ii) Connection is required to a particular outgoing highway, but any free Channel on it may be used (mode 2)	10
	b.	With flow diagram, discuss call forwarding feature.	6
		OR	
8	a.	With a neat diagram, explain the operation of time switch implementation and bilateral synchronization system.	8
	b.	Explain in brief, basic software architecture used in DSS.	8
		Module-5	
9	a.	Explain in brief the software process matrices and describe the defect analysis with an example.	10
	b.	Explain the concept of embedded patcher.	6
		OR	
10	a.	Explain in brief system outage and its impact on DSS reliability.	8
	b.	Explain in brief generic switch hardware architecture.	8

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MODEL QUESTION PAPER – Set II
6th Semester, B.E (CBCS) EC/TC

Course: 15EC654– Digital Switching Systems

Time: 3 Hours **Max Marks: 80**

Note: (i) Answer Five full questions selecting any one full question from each Module.
(ii) Question on a topic of a Module may appear in either its 1st or 2nd question.

		Module 1	
1	(a)	Explain different network structure used in communication.	8
	(b)	Explain with neat diagram four wire circuit.	8
		OR	
2	(a)	With a block schematic, explain the national telecommunication network.	8
	(b)	Explain the following power levels in dbm and dbw: (i) 1 mw (ii) 1w (iii) 2 mw (iii) 100 mw	4
	(c)	With suitable diagram explain the principle of frequency division multiplexing.	4
		Module 2	
3	(a)	Explain Message switching.	8
	(b)	Mention the functions of a switching systems	4
	(c)	Define (i) CCR (ii) BHCA (iii) Busy hour	4
		OR	
4	(a)	Explain the significance of distribution frames, with the help of neat diagram.	8
	(b)	With a neat diagram, explain basic call process of incoming and outgoing calls through digital switching systems.	8
		Module 3	
5	(a)	Derive the equation for finite queue capacity.	6

	(b)	During the busy hour a group of trunks is offered 100 calls having an average duration of 3 minutes, one of calls fails to find a disengaged trunk. Find the traffic offered to the group and the traffic carried by the group.	6
	(c)	Explain Business Ethics and Corporate Governance.	4
		OR	
6	(a)	Design a grading for connecting 20 trunks to switches having 10 outlets.	8
	(b)	Explain grading, Explain with a neat diagram, skipped and homogenous grading	8
		Module 4	
7	(a)	With neat sketch, explain space switch and time switch.	6
	(b)	Write a note on synchronization networks.	4
	(c)	Explain with a diagram classification of digital switching software	6
		OR	
8	(a)	Explain in brief basic software architecture used in digital switching system.	8
	(b)	With a neat sketch, explain the operation of a k x m space switch.	8
		Module 5	
9	(a)	Explain briefly with neat diagram of organizational interfaces of a typical digital switching systems central office.	8
	(b)	Explain in brief generic switch hardware architecture.	8
		OR	
10	(a)	Explain system outrage and its impact on digital switching system reliability.	6
	(b)	Write note on recovery strategy	4
	(c)	Draw a typical problem reporting system and explain function of each block	6

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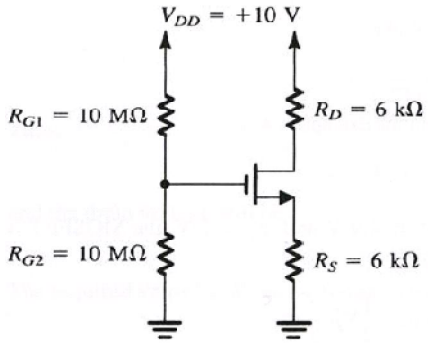
MODEL QUESTION PAPER – Set I

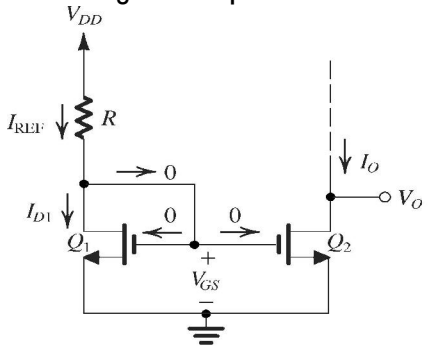
6th Semester, B.E (CBCS) EC

Course: 15EC655- Microelectronics

Time: 3 Hours **Max. Marks: 80**

Note: (i) Answer Five full questions selecting any one full question from each Module.
(ii) Question on a topic of a Module may appear in either its 1st or/and 2nd question.

		Module-1	Marks
1	a	With the neat diagram obtain the expression for finite output resistance in saturation region.	08
	b	Consider an NMOS transistor fabricated in a 0.18μm process with L = 0.18μm and W = 2μm. The process technology is specified to have C_{ox} =8.6 fF/μm^2, μ_n = 450cm^2/Vžs and V_m = 0.5V. i. Find V_{GS} and V_{DS} that results in the MOSFET operating at the edge of saturation with I_D = 100μA. ii. If V_{GS} is kept constant, find V_{DS} that results in I_D = 50μA	08
		OR	
2	a	With the neat diagram obtain the expression for drain current in various regions	08
	b	Analyze the circuit shown in figure Q.2b to determine the voltages at all nodes and the currents through all branches. Let V_{tn} = 1 V and $k'_n(W/L)$ = 1 mA/V^2. Neglect the channel length modulation effect.  Fig. Q.2b	06
		Module-2	
3	a	With the help of neat diagram explain the biasing of MOSFET by Fixing V_G with and without source resistance.	10
	b	Explain the small signal model of MOSFET and how the T equivalent-circuit model can be obtained.	06
		OR	
4	a	Explain the operation of MOSFET as an amplifier with necessary diagram	10

		expressions.	
	b	Explain the high frequency model of MOSFET with a neat diagram and internal capacitances.	06
		Module-3	
5	a	Explain the operation of MOS current steering circuit with necessary diagram and expressions.	08
	b	Given V_{DD} = 3V and using I_{REF} = 100μA, design the circuit shown in figure Q.5b to obtain an output current whose nominal value is 100μA. Find R if Q_1 and Q_2 are matched and have channel length of 1μm, channel widths of 10μm, V_t = 0.7 V and k'_n = 200μA/V^2. What is the lowest possible value of V_O? Assuming that for this process technology V'_A = 20V/μm, find the output resistance of the current source. Also find the change in output current resulting from a +1V change in V_O.  Fig. Q.5b	08
		OR	
6	a	With the help of a neat diagram and necessary expressions, explain the characteristic parameters of the common gate amplifier.	10
	b	Briefly explain Millers theorem.	06
		Module-4	
7	a	Explain the operation of common source amplifier with constant current load and obtain the necessary expression	08
	b	Find the midband gain A_M and the upper 3-dB frequency f_H of a CS amplifier fed with a signal source having an internal resistance R_{sig} = 100kΩ. The amplifier has R_G = 4.7MΩ, R_D = R_L = 15kΩ, g_m = 1mA/V, r_o = 150kΩ, C_{gs} = 1pF and C_{gd} = 0.4pF. Also find the frequency of the transmission zero.	08
		OR	
8	a	Explain the high frequency response of MOS Cascode amplifier with necessary diagram and expressions.	08
	b	Explain the operation of common gate amplifier with constant current load and obtain the necessary expression	08
		Module-5	
9	a	Explain the operation with a Commom-Mode input voltage of MOS differential pair	08
	b	Explain the small signal operation of MOS differential pair.	08
		OR	

10	a	Explain the frequency response of the MOS differential amplifier.	08
	b	Explain a Two stage CMOS Op-Amp.	08

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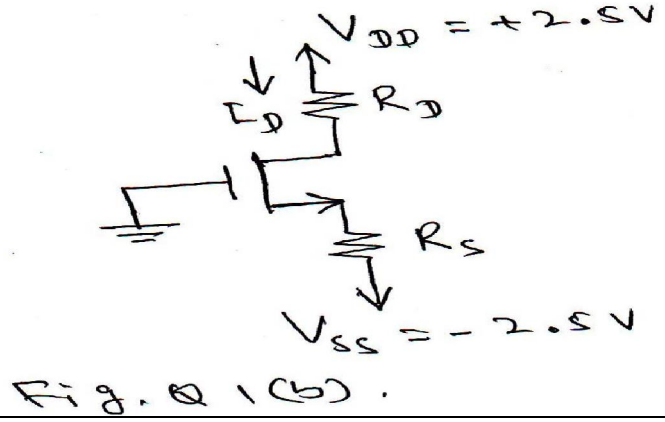
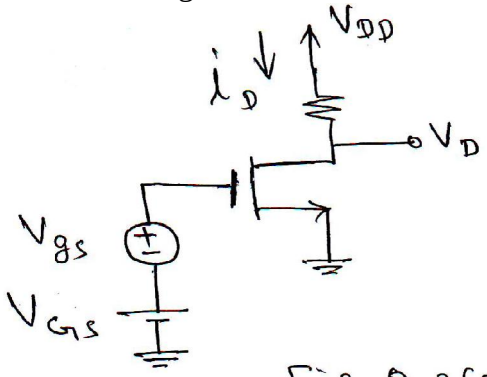
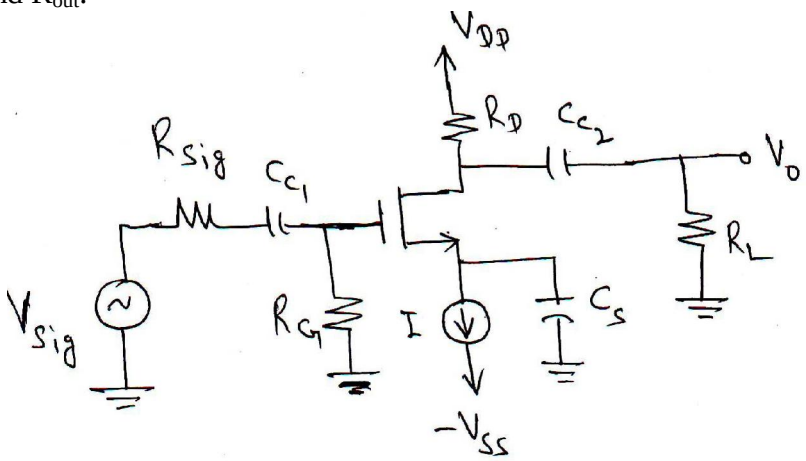
MODEL QUESTION PAPER – Set II
6th Semester, B.E (CBCS) EC

Course: 15EC655 - Microelectronics

Time: 3 Hours **Max. Marks: 80**

Note: (i) Answer Five full questions selecting any one full question from each Module.
(ii) Question on a topic of a Module may appear in either its 1st or/and 2nd question.

		MODULE 1	
1	a.	Derive the expression of drain current of a MOS device for triode and saturation region.	6 Marks
	b.	For the circuit shown in Fig. 1(b) has I_D = 0.4mA and V_D = 0.5V. The NMOS transistor has V_t = 0.7V, μnC_{OX} = 100μA/V^2, L = 1μm and W = 32μm. Find the values of Rs and R_D. Assume λ = 0.  Fig. Q 1(b).	6 Marks
	c.	Mention the advantages of MOSFETs.	4 Marks
		OR	
2	a.	Explain the operation of enhancement type NMOS transistor in detail.	8 Marks
	b.	Discus the role of substrate in the MOS with relevant equations. NMOS transistor has V_{to} = 0.8V, $2\phi_f$ = 0.7V and γ = 0.4V$^{1/2}$, find Vt when V_{SB} = 3V.	8 Marks
		MODULE - 2	
3	a.	Draw the T – equivalent circuit model for the MOSFET and explain.	6 Marks
	b.	Explain the biasing of the MOSFET using constant current source.	6 Marks

	c.	Derive the expression of $A_V = -g_m R_D$ for the circuit shown in Fig. 3(c).  Fig. Q 3(c)	4 Marks
		OR	
4	a.	For the circuit shown in Fig. 4(a), obtain the expressions of R_{in}, A_V, A_{VO}, G_V and R_{out}.  Fig. Q 4(a)	8 Marks
	b.	Explain the role of various internal capacitances in the MOSFET.	8 Marks
		MODULE - 3	
5	a.	For an NMOS transistor with W/L = 10 fabricated in the 0.18µm process, find the values of V_{OV} and V_{GS} required to operate the device at I_D = 100µA. Ignore channel length modulation. Assume $\mu_n C_{OX} = 387\mu A/V^2$.	6 Marks
	b.	Explain the operation of a basic MOSFET current mirror.	5 Marks
	c.	State and prove the Miller's Theorem.	5 Marks
		OR	
6	a.	Draw and explain the circuit for generating the number of constant currents of various magnitude of a current steering.	8 Marks
	b.	Derive the expression for determining the 3-dB frequency (ω_H) of an amplifier.	8 Marks
		MODULE - 4	
7	a.	Draw the circuit diagram of a CMOS Common Source amplifier and explain its operation with the help of I-V characteristics and transfer	8 Marks

		characteristics.	
	b.	Explain what is Cascode amplifier and the basic idea behind the Cascode amplifier.	4 Marks
	c.	Explain the operation of a Double Cascoding.	4 Marks
OR			
8	a.	Draw the high frequency equivalent circuit model of the common source amplifier and explain the analysis using open circuit time constants.	8 Marks
	b.	Explain the effect of source resistance on transconductance and voltage gain of a CS- amplifier.	8 Marks
MODULE - 5			
9	a.	Explain the operation of MOS differential pair with a differential input voltage.	8 Marks
	b.	Obtain the expression of CMRR of an active loaded MOS differential amplifier.	8 Marks
OR			
10	a.	Draw the diagram of a two stage CMOS op-amp circuit and explain its operation.	8 Marks
	b.	Draw the frequency response of a differential amplifier due to variation of common - mode gain, differential gain and CMRR with frequency and analyse it.	8 Marks

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