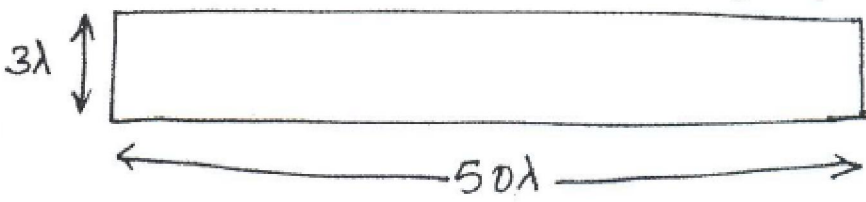**Visvesvaraya Technological University, Belagavi**
MODEL QUESTION PAPER- Set I
6th Semester, B.E (CBCS) ECE

Course: 15EC63- VLSI DESIGN

Time: 3 Hours   **Max. Marks: 80**

Note: (i) Answer five full questions selecting any one full question from each Module.

(ii) Question on a topic of a Module may appear in either its 1st or/and 2nd question.

			Module-1	Marks
1	a		What do you mean by static load inverters? Derive the output voltage for pseudo Inverter by discussing its dc characteristics.	8
	b		Derive the CMOS inverter DC characteristics graphically from p device and n device characteristics and show all operating regions.	8
			OR	
2	a		Explain the nMOS enhancement mode transistor operation for different values of V_{gs} and V_{ds} .	6
	b		Explain the fabrication steps of CMOS p-well process with neat diagram and write the mask sequence.	6
	c		What are the advantages of BiCMOS process over CMOS technology.	4
			Module-2	
3	a		Explain based design rules with neat diagram.	6
	b		Draw the circuit and stick diagram for nMOS and CMOS implementation of Boolean expression = +	10
			OR	
4	a		Calculate the capacitance in C_g for the given metal layer shown in the Fig Q4(a), if feature size=5µm and relative value of metal to substrate =0.075.	8

Fig Q4(a)

	b		Define sheet resistance R_s and standard unit of capacitance (C_g). Calculate the on resistance of 4:1 nMOS inverter with R_s=10k / , Z_{pu}=8 /2 , Z_{pd}=2 /2 . Also	8

		estimate the total power dissipated if $V_{DD}=5V$.	
		Module-3	

5	a	Find the scaling factors for:
		    i) Saturation current
		    ii) Current density
		    iii) Power dissipation/unit area
		    iv) Maximum operating frequency
			8

	b	Design a 4 bit ALU to implement addition, subtraction, EX-OR, EX-NOR, OR and AND operations.	8
		OR	
6	a	With a neat diagram, explain 4x4 barrel shifter.	8
	b	Describe Manchester Carry-chain.	8
		Module-4	
7	a	Discuss the architectural issues related to subsystem.	8
	b	Explain Pseudo nMOS logic for NAND gate and Inverter.	8
		OR	
8	a	Explain Parity generator with basic block diagram and stick diagram.	8
	b	Explain FPGA architectures.	8
		Module-5	
9	a	Explain 3 transistor dynamic RAM cell.	8
	b	Write a note on testability and testing.	8
		OR	
10	a	Explain the scan design techniques.	8
	b	Demonstrate write operation & read operation for four transistor dynamic and six transistor static CMOS memory cell.	8

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