Visvesvaraya Technological University, Belagavi

MODEL QUESTION PAPER – Set I

6th Semester, B.E (CBCS) EC

Course: 15EC655- Microelectronics

Time: 3 Hours   Max. Marks: 80

Note: (i) Answer Five full questions selecting any one full question from each Module.

   (ii) Question on a topic of a Module may appear in either its 1st or/and 2nd question.

		Module-1	Marks
1	a	With the neat diagram obtain the expression for finite output resistance in saturation region.	08
	b	Consider an NMOS transistor fabricated in a 0.18μm process with L = 0.18μm and W = 2μm. The process technology is specified to have C_{ox} =8.6 fF/μm^2, μ_n = 450cm^2/Vžs and V_m = 0.5V. i. Find V_{GS} and V_{DS} that results in the MOSFET operating at the edge of saturation with I_D = 100μA. ii. If V_{GS} is kept constant, find V_{DS} that results in I_D = 50μA	08
		OR	
2	a	With the neat diagram obtain the expression for drain current in various regions	08
	b	Analyze the circuit shown in figure Q.2b to determine the voltages at all nodes and the currents through all branches. Let V_{tn} = 1 V and k $_n$(W/L) = 1 mA/V^2. Neglect the channel length modulation effect. Fig. Q.2b	06
		Module-2	
3	a	With the help of neat diagram explain the biasing of MOSFET by Fixing V_G with and without source resistance.	10
	b	Explain the small signal model of MOSFET and how the T equivalent-circuit model can be obtained.	06
		OR	
4	a	Explain the operation of MOSFET as an amplifier with necessary diagram	10

		expressions.	
	b	Explain the high frequency model of MOSFET with a neat diagram and internal capacitances.	06
		Module-3	
5	a	Explain the operation of MOS current steering circuit with necessary diagram and expressions.	08
	b	Given $V_{DD} = 3V$ and using $I_{REF} = 100\mu A$, design the circuit shown in figure Q.5b to obtain an output current whose nominal value is $100\mu A$. Find R if Q_1 and Q_2 are matched and have channel length of $1\mu m$, channel widths of $10\mu m$, $V_t = 0.7$ V and $k_n = 200\mu A/V^2$. What is the lowest possible value of V_O? Assuming that for this process technology $V_A = 20V/\mu m$, find the output resistance of the current source. Also find the change in output current resulting from a +1V change in V_O. Fig. Q.5b	08
		OR	
6	a	With the help of a neat diagram and necessary expressions, explain the characteristic parameters of the common gate amplifier.	10
	b	Briefly explain Millers theorem.	06
		Module-4	
7	a	Explain the operation of common source amplifier with constant current load and obtain the necessary expression	08
	b	Find the midband gain A_M and the upper 3-dB frequency f_H of a CS amplifier fed with a signal source having an internal resistance $R_{sig} = 100k\Omega$. The amplifier has $R_G = 4.7M\Omega$, $R_D = R_L = 15k\Omega$, $g_m = 1mA/V$, $r_o = 150k\Omega$, $C_{gs} = 1pF$ and $C_{gd} = 0.4pF$. Also find the frequency of the transmission zero.	08
		OR	
8	a	Explain the high frequency response of MOS Cascode amplifier with necessary diagram and expressions.	08
	b	Explain the operation of common gate amplifier with constant current load and obtain the necessary expression	08
		Module-5	
9	a	Explain the operation with a Commom-Mode input voltage of MOS differential pair	08
	b	Explain the small signal operation of MOS differential pair.	08
		OR	

10	a	Explain the frequency response of the MOS differential amplifier.	08
	b	Explain a Two stage CMOS Op-Amp.	08