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Model Question Paper-1 with effect from 2019-20 (CBCS Scheme)

USN **18EE46** | | | | | | | | | |

Fourth Semester(CBCS)B.E.DegreeExamination
OPERATIONAL AMPLIFIERS AND LINEAR ICs

TIME: 03 Hours **Max. Marks: 100**

Note: 01. Answer any **FIVE** full questions, choosing at least **ONE** question from each **MODULE**.

			Bloom's Taxonomy Level	Marks
		Module 1		
Q. 01	**a**	**Explain the characteristics of an ideal op-amp and compare ideal and practical op-amp.**	**L2**	**(08)**
	b	**Explain the virtual ground concept.**	**L2**	**(06)**
	C	**Explain the operation of the difference amplifier circuit and derive an equation for the output voltage.**	**L2**	**(06)**
		OR		
Q. 02	**a**	**Design a suitable non inverting amplifier circuit which is to amplify a 100mV signal to level of 3V using a 741 op-amp.**	**L3**	**(06)**
	b	**Explain the operation of differential input/output amplifier and derive an equation for voltage gain.**	**L2**	**(08)**
	c	**Explain the operation of capacitor coupled non-inverting AC amplifier.**	**L2**	**(06)**
		Module 2		
Q. 03	**a**	**Derive the gain equation for first order low pass Butterworth filter.**	**L3**	**(06)**
	b	**List the various filters classifications according to the frequency response sketch approximate Av/f graphs for each type.**	**L1**	**(08)**
	c	**A first order low –pass filter with C_1=0.01μF has R_1 consisting of a 3.3KΩ resistor in series with a1KΩ variable resistor calculate the maximum and minimum cut off frequency.**	**L3**	**(06)**
		OR		
Q. 04	**a**	**An unregulated D.C power supply output changes from 20V to 19.7V when the load is increased from zero to maximum the voltage also increases to 20.2V when the A.C supply increase by 10.7.calculate the load and source effects and the load and line regulations.**	**L3**	**(07)**
	b	**Explain the operation of op-amp series voltage regulator with neat circuit diagram.**	**L2**	**(07)**
	c	**Explain the working of adjustable output regulator with neat circuit diagram.**	**L2**	**(06)**

		Module 3	Bloom's Taxonomy Level	Marks
Q. 05	a	Explain the oscillator amplitude stabilization with necessary figures.	L2	(08)
	b	Explain the working of current to voltage converter with grounded load.	L2	(06)
	C	Explain the sawtooth wave oscillator with a neat circuit diagram.	L2	(06)
		OR		
Q. 06	a	Design a non inverting Schmitt trigger circuit to have LTP= -1.5V and UTP=1V.	L2	(07)
	b	Explain the working and design of RC phase shift oscillator with neat circuit diagram.	L2	(07)
	c	Discuss the basics of voltage to frequency and frequency to voltage converters.	L3	(06)
		Module 4		
Q.07	a	Design a precision full wave rectifier to produce 2V peak output from sine wave input of peak value 0.5V and frequency of 1MHz, use 741 op-amp with ±12V supply.	L3	(08)
	b	Explain the LSB and the MSB in a digital code.	L2	(06)
	c	A 500mV level is to be converted into a7-bit digital code. Determine the resolution of the conversion the analog levels represented by the LSB and the MSB and calculate the analog level represented by 1111111.	L2	(06)
		OR		
Q.08	a	Discuss how the DAC can be used to convert an input in digital code into analog form.	L2	(07)
	b	Explain the circuit operation of a saturating type half wave precision rectifier Draw its input and output waveform.	L2	(07)
	c	Explain the working of integrated circuit 8 bit DAC.	L3	(06)
		OR		
Q.09	a	Explain the internal architecture of IC555 timer with a neat diagram.	L2	(08)
	b	Write a note on applications of PLL.	L1	(06)
	c	A PLL system with a 105KHz input has a VCO with a 100KHz free-running frequency and 3.3kHz /V sensitivity. The phase detector sensitivity is 0.68V/rad and the amplifier gain is 5. Calculate the loop gain, the input/output, phase difference.	L3	(06)
		OR		
Q.10	a	Sketch the block diagram for a basic PLL system together with the system waveforms.	L2	(06)
	b	Design a mono stable circuit using a741 op-amp with a ±18V supply that produces a400Hz output frequency.	L3	(08)
	c	Define VCO, sensitivity free-running frequency.	L1	(06)