# Model Question Paper-1 with effect from 2019-20 (CBCS Scheme)

USN | | | | | | | | | | |

## Fourth Semester B.E. Degree Examination

## Operational Amplifiers and Linear ICs

**TIME: 03 Hours** **Max. Marks: 100**

Note: 01. Answer any **FIVE** full questions, choosing at least **ONE** question from each **MODULE**.

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| | | **Module -1** | |
| Q.01 | a | Define the following terms 1) Input offset current 2) Input offset voltage 3) Differential gain 4)CMRR | 06 |
| | b | Draw the block diagram of Op Amp and Explain. | 08 |
| | c | Determine the output voltage in each of the following cases for the open loop differential Amplifier.<br>1)$V_{in1}$=5μv DC, Vin2=-7μv DC<br>2)$V_{in1}$=10mV RMS, Vin2=10mV RMS, Op amp is a 741 with the following specifications A=200000,Ri=2MΩ ,R0=75Ω,Vcc=±15V & output voltage swing=±14V | 06 |
| | | OR | |
| Q.02 | a | Explain inverting and non-inverting configuration of summing Amplifier. | 08 |
| | b | The circuit of peaking amplifier is to provide the gain of 10 at a peak frequency of 16kHz.determine the values of all the components. | 06 |
| | c | What is an instrumentation Amplifier? With the neat circuit diagram explain the operation of the same. | 06 |
| | | **Module-2** | |
| Q. 03 | a | With the neat circuit diagram explain second order low pass Butterworth filter. Derive the expression for the gain of the filter. | 10 |
| | b | Design a wide band pass filter having $F_L$=600Hz and $F_H$=4kHz and the pass band gain of 6. Assume the capacitor value of high pass & low pass filter as 0.05μF & 0.01μF respectively, draw the frequency response of the filter and also calculate the Q value of the filter. | 06 |
| | c | State the difference between Active and Passive filters. | 04 |
| | | OR | |
| Q.04 | a | Define the following terms 1)Load regulation 2) Line regulation 3)voltage stability factor 4) Ripple rejection | 06 |
| | b | An voltage follower regulator has $V_S$=12V,$V_0$=6.3V,$R_1$=270 Ω & $I_{L(Max)}$=42mA. If the supply source resistance is 25 Ω determine 1) Line regulation 2) Load regulation 3) Ripple rejection for the circuit. | 06 |
| | c | Write a short note on 1) LM317 2) LM337 IC regulators. | 08 |
| | | **Module-3** | |
| Q. 05 | a | With the neat diagram explain the operation of Triangular /Rectangular wave generator. | 06 |
| | b | Explain the operation of RC phase shift oscillator. Deduce the expression for frequency and gain for the same. | 10 |
| | c | What is oscillator amplitude stabilization? Explain the same in case of Wien bridge oscillator. | 04 |
| | | OR | |
| Q. 06 | a | Explain with the neat circuit diagram & waveform the operation of Inverting and non-inverting Zero crossing detector. | 08 |
| | b | Explain with the neat circuit diagram & waveform the operation of Inverting and non-inverting regenerative comparator. | 08 |
| | c | With the neat circuit diagram, Voltage to Current converter with grounded load. | 04 |

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| | | **Module-4** | |
| Q. 07 | a | What are the major limitations of conventional rectifier? Explain the operation of precision full wave rectifier as a combination of half wave rectifier and a summing circuit. | 08 |
| | b | Design a precision full wave rectifier to produce 2V peak output voltage from a sine wave input of peak value 0.5V and frequency of 1MHz, use 741 op-amp with ±12V supply. | 06 |
| | c | Explain the principle of operation of R-2R ladder digital to analog converter with the neat diagram. | 06 |
| | | OR | |
| Q. 08 | a | Explain integrated circuit 8- bit digital to analog converter with the necessary diagrams. | 07 |
| | b | Explain the working of ADC using successive approximation method. | 07 |
| | c | Explain the working principle of linear RAMP analog to digital converter. | 06 |
| | | **Module-5** | |
| Q. 09 | a | Explain the operating principle of PLL. Hence define lock range, capture range & pull in time. | 10 |
| | b | Explain how XOR gates can be used as phase detector in PLL. | 05 |
| | c | Explain monostable multivibrator, realized using IC555 timer. | 05 |
| | | OR | |
| Q. 10 | a | With a neat diagram, explain the internal architecture of IC555 timer. | 06 |
| | b | An astable multivibrator is to be designed for getting rectangular waveform for $T_{ON}$=0.6ms. Total time period =1ms.Assume C=0.1μ F Draw the circuit diagram. | 06 |
| | c | Explain PLL IC565 application as frequency multiplier and frequency synthesizer. | 08 |