Model Question Paper -1 with effect from 2020-21(CBCS Scheme)

USN | | | | | | | | | | |

Fifth Semester B.E. Degree Examination
Verilog HDL (18EC56)

TIME: 03 Hours **Max. Marks: 100**

Note: 01. Answer any **FIVE** full questions, choosing at least **ONE** question from each **MODULE**.

Module – 1			
Q.1	**(a)**	Explain design flow for designing VLSI IC circuits with a neat flowchart.	10m
	(b)	List the importance of HDL. Mention the two popular HDLs.	(4+2)m
	(c)	How is Verilog different from High level language.	4m
OR			
Q.2	**(a)**	Discuss the different levels of abstraction used in Verilog modelling.	8m
	(b)	What is stimulus? Explain different types of stimulus block instantiation.	(1+7)m
	(c)	Describe the digital system design using hierarchical design methodologies.	4m
Module – 2			
Q.3	**(a)**	List all the data types available in Verilog HDL. Explain any three data types with examples.	(2+6)m
	(b)	Explain the port connection rules of Verilog HDL with examples.	6m
	(c)	Bring out the difference between $display and $monitor with an example.	6m
OR			
Q.4	**(a)**	What are the components of SR latch? Write Verilog HDL module of SR latch and test bench to verify the SR Latch	(2+3+3)m
	(b)	Explain with example how sized and unsized numbers are represented in Verilog.	6m
	(c)	Describe different methods of connecting ports to external signals.	6m
Module – 3			
Q.5	**(a)**	A=5'b10101, B=5'b11111, C=5'b11000, D= 5'b10001. Evaluate i.A&B ii. C^^D iii B % D iv. B<<2 v. !(&A) vi. Y=(A>=B) vii. Y= {A[2], B[0], C} viii. y=(A > B): 1:0	8m

	(b)	Mention the symbol, truth table and an example for following primitives i. BUFIF1 ii, NOTIF0 iii. AND	6m
	(c)	Write a Verilog code to realize 2-bit comparator (A1A0 & B1B0) in gate level to give the outputs AequalB, AgreaterthanB, AlesserthanB. Verify the code with an appropriate test bench.	6m
OR			
Q.6	**(a)**	Explain Carry Look Ahead adder. Write a Verilog code with data flow style program for carry look ahead adder.	10m
	(b)	What is continuous assignment? Discuss the rules of continuous assignment.	6m
	(c)	Write a Verilog code for 4X1 MUX using conditional operators.	4m
Module – 4			
Q.7	**(a)**	Differentiate i. always and initial procedural statements ii. blocking and non-blocking statements.	8m
	(b)	Explain the following control statement with an example. i. if …else statement ii. For loop.	6m
	(c)	Write a Verilog code to generate the following sequence 1,2,4,6,7,1,2…. Verify the code with an appropriate test bench.	6m
OR			
Q.8	**(a)**	Bring out the difference between task and functions.	6m
	(b)	Write Verilog program to call a function called calc_parity which computes the parity of a 32-bit data, [31-0]Data and display odd or even parity message.	8m
	(c)	Compare parallel and sequential blocks with an example.	6m
Module – 5			
Q.9	**(a)**	What is parameter overriding and why it is needed? Discuss different techniques of parameter overriding with an example for each.	8m
	(b)	Explain the "force and release" statement with an example. How is it different from assign.	8m
	(c)	Discuss the system tasks related to files.	4m
OR			
Q.10	**(a)**	Define the term logic synthesis.	2m
	(b)	With a neat flow chart explain Computer-Aided logic synthesis process.	10m

	(c)	What will the following statement translate to when run on a logic synthesis tool.
		i. assign y= (a&b) | (c&d) where out, a, b, c, d are 3 bit vectors
		ii. if (s)
		out=i1;
		else
		out=i0;
			8m

Table showing the Bloom's Taxonomy Level, Course Outcome and Programme Outcome				
Question		**Bloom's Taxonomy Level attached**	**Course Outcome**	**Programme Outcome**
Q.1	(a)	L2,L4	CO3	
	(b)	L2	CO3	
	(c)	L2	CO3	
Q.2	(a)	L1, L2	CO3	
	(b)	L1	CO2	
	(c)	L1, L2	CO3	
Q.3	(a)	L1, L2	CO1, CO2	
	(b)	L1	CO3	
	(c)	L4	CO4	
Q.4	(a)	L1,L3	CO1,CO2	
	(b)	L1	CO1	
	(c)	L2	CO2	
Q.5	(a)	L3	CO1	
	(b)	L2	CO2	
	(c)	L3	CO1,CO2	
Q.6	(a)	L1,L4	CO1	
	(b)	L1	CO1	
	(c)	L3	CO1	
Q.7	(a)	L4	CO1	
	(b)	L1	CO1	
	(c)	L3	CO1,CO2	
Q.8	(a)	L2	CO4	
	(b)	L3	CO4	
	(c)	L2	CO1	
Q.9	(a)	L1, L2	CO4	
	(b)	L1. L2	CO4	
	(c)	L1	CO4	
Q.10	(a)	L2	CO5	
	(b)	L1,L4	CO5	
	(c)	L3	CO5	

Bloom's Taxonomy Levels	**Lower order thinking skills**		
	Remembering(knowledge):L_1	Understanding Comprehension): L_2	Applying (Application): L_3
	Higher order thinking skills		
	Analyzing (Analysis): L_4	Valuating (Evaluation): L_5	Creating (Synthesis): L_6