Model Question Paper -1 with effect from 2020-21(CBCS Scheme)

USN

Fifth Semester B.E. Degree Examination
VLSI Design

TIME: 03 Hours   **Max. Marks: 100**

Note: 01. Answer any **FIVE** full questions, choosing at least **ONE** question from each **MODULE**.
         02.
         03.

		Module – 1	
Q.1	**(a)**	How moor's law can be related to evolution of microelectronics?	4
	(b)	With neat diagram explain the fabrication of nMOS transistor.	10
	(c)	Distinguish between CMOS and Bipolar technologies.	6
		OR	
Q.2	**(a)**	Derive an expression for an nMOS inverter in non-saturation and saturation region. Draw the relevant sketches.	10
	(b)	What is body effect in MOS transistors and how it affects the MOS transistor threshold voltage?	5
	(c)	Derive the expression for transconductance of MOS transistor.	5
		Module – 2	
Q.3	**(a)**	Derive the pull up to pull down ratio for an nMOS inverter, driven through, one or more pass transistors.	10
	(b)	With relevant sketches analyze the different operating regions of CMOS inverter.	10
		OR	
Q.4	**(a)**	Define the sheet resistance. How the sheet resistance can be calculated for the MOS transistor and inverter?	10
	(b)	What are the problems associated with MOS transistor to drive large capacitive load? What are the different techniques available to drive large capacitive loads? Obtain the expression for the overall delay T_d for cascaded inverters.	10
		Module – 3	
Q.5	**(a)**	Illustrate the stick diagram of one-bit shift register cell using CMOS design style with step by step procedure.	10
	(b)	What is the lambda-based design rules for the wires and transistors in nMOS and CMOS technology?	10

		OR	
Q.6	**(a)**	Derive the following scaling factors: (i) Gate Area A_g (ii) Gate Delay T_d (iii) Maximum operating frequency f_0 (iv) Switching energy per gate E_g (v) Gate capacitance C_g	10
	(b)	What are the limitations of scaling in VLSI technology? Discuss the effect of any two limitations of scaling.	10
		Module – 4	
Q.7	**(a)**	Draw the circuit diagram and stick diagram for 2 i/p NAND gate using NMOS and CMOS.	10
	(b)	Design a general logic function block to generate any function of two variables (A,B) using four way multiplexer.	10
		OR	
Q.8	**(a)**	Explain the general arrangement of a 4-bit arithmetic processor and basic bus architectures.	10
	(b)	Illustrate the generation of two-phase clock signals using D flip flops along with its waveforms.	6
	(c)	Describe the operation of active bus and passive bus arrangements for bus lines.	4
		Module – 5	
Q.9	**(a)**	Define regularity	2
	(b)	Write the expressions for a carry look ahead adders. Draw and explain the structure.	10
	(c)	Explain the serial parallel multiplier with D-flip-tlop and full adder.	8
		OR	
Q.10	**(a)**	Describe the operation of three transistor dynamic RAM cell and also write its stick diagram	8
	(b)	What are to be considered in the designer 's tool box for the chip design in CAD tools and explain simulation?	12

Table showing the Bloom's Taxonomy Level, Course Outcome and Programme Outcome				
Question		**Bloom's Taxonomy Level attached**	**Course Outcome**	**Programme Outcome**
Q.1	(a)	L1	CO1	PO1
	(b)	L2	CO1	PO1
	(c)	L2	CO1	PO1
Q.2	(a)	L2	CO2	PO1, PO2
	(b)	L2	CO2	PO1, PO2
	(c)	L2	CO2	PO1, PO2
Q.3	(a)	L3	CO2	PO1, PO2, PO3
	(b)	L3	CO2	PO1, PO2, PO3
Q.4	(a)	L3	CO2	PO1, PO2, PO3
	(b)	L3	CO2	PO1, PO2, PO3
Q.5	(a)	L3	CO3	PO1, PO2, PO3
	(b)	L1	CO2	PO1, PO2
Q.6	(a)	L2	CO2	PO1, PO2
	(b)	L2	CO2	PO1, PO2
Q.7	(a)	L2	CO3	PO1, PO2, PO3
	(b)	L3	CO3	PO1, PO2, PO3
Q.8	(a)	L2	CO3	PO1, PO2, PO3
	(b)	L2	CO3	PO1, PO2
	(c)	L2	CO3	PO1, PO2
Q.9	(a)	L1	CO4	PO1
	(b)	L2	CO4	PO1, PO2
	(c)	L2	CO4	PO1, PO2
Q.10	(a)	L2	CO4	PO1, PO2
	(b)	L1	CO5	PO1, PO2, PO3

Bloom's Taxonomy Levels	**Lower order thinking skills**		
	Remembering(knowledge):L_1	Understanding Comprehension): L_2	Applying (Application): L_3
	Higher order thinking skills		
	Analyzing (Analysis): L_4	Valuating (Evaluation): L_5	Creating (Synthesis): L_6

Model Question Paper -2 with effect from 2020-21(CBCS Scheme)

USN

Fifth Semester B.E. Degree Examination
VLSI Design

TIME: 03 Hours   **Max. Marks: 100**

Note: 01. Answer any **FIVE** full questions, choosing at least **ONE** question from each **MODULE**.
02.
03.

		Module – 1	
Q.1	**(a)**	Identify a suitable VLSI technology for optimum speed and power performance.	4
	(b)	Describe with neat sketches, the fabrication of P – well CMOS inverter.	10
	(c)	With neat sketches describe the working of enhancement mode transistor.	6
		OR	
Q.2	**(a)**	What are the aspects of MOS transistor threshold voltage?	8
	(b)	Derive the expression for transconductance and output conductance of MOS transistor.	8
	(c)	Draw the MOS transistor characteristics curve in enhancement mode and depletion mode.	4
		Module – 2	
Q.3	**(a)**	Derive the pull up to pull down ratio for an nMOS inverter driven through another nMOS inverter.	8
	(b)	Analyze the latch up in CMOS Circuits with relevant sketches and mention the remedies to overcome latch up.	8
	(c)	List the alternate forms of pull ups along with its characteristic graph.	4
		OR	
Q.4	**(a)**	Estimate the rise time and fall time of a CMOS inverter.	8
	(b)	Justify that BiCMOS inverters can drive large capacitive loads with lesser delay than compared to CMOS inverter with relevant sketches and graphs.	8
	(c)	Explain the working of inverting super buffers?	4
		Module – 3	
Q.5	**(a)**	Draw the stick diagram of n-well based BiCMOS inverter.	6
	(b)	Using nMOS design style draw the stick diagram of the Boolean equation X` A + BC	8
	(c)	What is the lambda-based design rules for the transistors in nMOS, pMOS and CMOS technology?	6

		OR	
Q.6	**(a)**	Derive the following scaling factors: (i) Gate capacitance per unit area C_o (ii) Carrier density in channel Q_{on} (iii) Saturation current I_{dss} (iv) Switching energy per gate Eg (v) Current density J	10
	(b)	Discuss the limitations of scaling with respect to following parameters. (i) Substrate doping scaling factor (ii) Limits of miniaturization	10
		Module – 4	
Q.7	**(a)**	Draw the circuit diagram and stick diagram for 2-i/p nor gate in nMOS and CMOS family	10
	(b)	Explain bus arbitration logic for n-line bus moving from unstructured design to structured design.	10
		OR	
Q.8	**(a)**	Draw and describe the working of NMOS version of dynamic shift register.	6
	(b)	Discuss the working of 4 x 4-barrel shifter with the neat circuit diagram and stick diagram.	8
	(c)	What are the general considerations in VLSI design methodology	6
		Module – 5	
Q.9	**(a)**	Implement a 4 bit ALU using a 4 bit adder	10
	(b)	Explain the 2's compliment multiplication using the Baugh-Wooley method.	10
		OR	
Q.10	**(a)**	Describe the read and write operations in static RAM with neat diagram.	10
	(b)	With the help of circuit diagram explain the operation of the following (i) JK Flipflop (ii) D Flipflop	10

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Bloom's Taxonomy Levels	\multicolumn{3}{c	}{Lower order thinking skills}	
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	\multicolumn{3}{c	}{Higher order thinking skills}	
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